**GigaDevice Semiconductor Inc.**

**GD32F470xx**

**Arm® Cortex®-M4 32-bit MCU**

Datasheet

Revision 2.1 (Jan. 2025)

GD32F470xx Datasheet

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**1.**

**General description**

The GD32F470xx device belongs to the stretch performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features a Floating Point Unit (FPU) that accelerates single precision floating point math operations and supports all Arm® single precision instructions and data types. It implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F470xx device incorporates the Arm® Cortex®-M4 32-bit processor core operating at 240 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 3072 KB on-chip Flash memory and 768 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2.6 MSPS ADCs, two 12-bit DACs, up to eight general 16-bit timers, two 16- bit PWM advanced timers, two 32-bit general timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to six SPIs, three I2Cs, four USARTs and four UARTs, two I2Ss, two CANs, a SDIO, USBFS and USBHS, and an ENET. Additional peripherals as Digital camera interface (DCI), EXMC interface with SDRAM extension support, TFT-LCD Interface (TLI) and Image Processing Accelerator (IPA) are included.

The device operates from a 2.6 to 3.6V power supply and available in -40 to +85 °C temperature range for grade 6 devices, and -40 to 105 °C temperature range for grade 7 devices. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F470xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, automotive navigation, drone, IoT and so on.

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**2.** **Device overview**

**2.1.**

**Device information**

**Table 2-1. GD32F470xx devices features and peripheral list**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Part**  **Number** | | **GD32F470xx** | | | | | | | | | | | | | |
| **VE** | **VG** | **VI** | **VK** | **VG** | **VI** | **VK** | **ZE** | **ZG** | **ZI** | **ZK** | **IG** | **II** | **IK** |
|  | **Code area (KB)** | 512 | 768 | 512 | 1024 | 768 | 512 | 1024 | 512 | 768 | 512 | 1024 | 768 | 512 | 1024 |
| **Data area (KB)** | 0 | 256 | 1536 | 2048 | 256 | 1536 | 2048 | 0 | 256 | 1536 | 2048 | 256 | 1536 | 2048 |
| **Total**  **(KB)** | 512 | 1024 | 2048 | 3072 | 1024 | 2048 | 3072 | 512 | 1024 | 2048 | 3072 | 1024 | 2048 | 3072 |
| **SRAM (KB)** | | 256 | 512 | 768 | 256 | 512 | 768 | 256 | 256 | 512 | 768 | 256 | 512 | 768 | 256 |
|  | **General**  **timer(16**  **-bit)** | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) | 8  (2-3,8-13) |
| **General**  **timer(32**  **-bit)** | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) | 2  (1,4) |
| **Advanc**  **ed**  **timer(16**  **-bit)** | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) | 2  (0,7) |
| **Basic**  **timer(16**  **-bit)** | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) | 2  (5,6) |
| **SysTick** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **Watchd**  **og** | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| **RTC** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
|  | **USART** | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| **UART** | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| **I2C** | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| **SPI/I2S** | 5/2  (0-4)/(1-2) | 5/2  (0-4)/(1-2) | 5/2  (0-4)/(1-2) | 5/2  (0-4)/(1-2) | 5/2  (0-4)/(1-2) | 5/2  (0-4)/(1-2) | 5/2  (0-4)/(1-2) | 6/2  (0-5)/(1-2) | 6/2  (0-5)/(1-2) | 6/2  (0-5)/(1-2) | 6/2  (0-5)/(1-2) | 6/2  (0-5)/(1-2) | 6/2  (0-5)/(1-2) | 6/2  (0-5)/(1-2) |
| **SDIO** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

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3(16) 3(16) 3(16) 3(16) 3(16) 3(16) 3(16) 3(24) 3(24) 3(24) 3(24) 3(24) 3(24) 3(24)

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**2.2.**

**Block diagram**

**Figure 2-1. GD32F470xx block diagram**

Powered By LDO (1.2V)

Flash Memory

TPIU SW/JTAG master

slave

FMC

ARM Cortex-M4 master slave Powered By VDDA

Processor

Fmax: 240MHz

master

slave

slave

TCMSRAM

SRAM0

DAC

LVD PLLs

DMA0

DMA1

ENET

M

P

M

P

master

master

master

master

master

slave slave slave slave

SRAM1

SRAM2

ADDSRAM

EXMC

IRC16M

IRC32K

BKPSRAM CRC GPIO RCU

TLI master slave

AHB1 Peripherals

USBHS master

TRNG DCI USBFS

slave

IPA master AHB2 Peripherals

AHB Interconnect Matrix (Fmax=240MHz)

EXTI SDIO SPI5 SPI4 SPI3 SPI0

ADC0~2

SYSCFG TIMER10 TIMER9 TIMER8 TIMER7 TIMER0 USART5 USART0

CTC

IREF TIMER13 TIMER12 TIMER11 TIMER6 TIMER5 TIMER4 TIMER3 TIMER2 TIMER1 WWDGT

DAC0 CAN1 CAN0 UART7 UART6 UART4 UART3 USART2 USART1

I2C2 I2C1 I2C0

SAR

ADC

Powered By VDDA

POR/ PDR

LDO

I2S2\_add SPI2/I2S2 SPI1/I2S1

FWDGT I2S1\_add

HXTAL PMU

LXTAL

Powered By VDD

RTC

Powered By VBAT

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**2.3.**

**Pinouts and pin assignment**

**Figure 2-2. GD32F470Ix BGA176 pinouts**

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

A PE3 PE2 PE1 PE0 PB8 PB5 PG14 PG13 PB4 PB3 PD7 PC12 PA15 PA14 PA13

B PE4 PE5 PE6 PB9 PB7 PB6 PG15 PG12 PG11 PG10 PD6 PD0 PC11 PC10 PA12

C VBAT PI7 PI6 PI5 VDD PDR\_ON VDD VDD VDD PG9 PD5 PD1 PI3 PI2 PA11

D PC13 PI8 PI9 PI4 VSS BOOT0 VSS VSS VSS PD4 PD3 PD2 PH15 PI1 PA10

E PC14 PF0 PI10 PI11 PH13 PH14 PI0 PA9

F

G

PC15

PH0/O SCIN

VSS

VSS

VDD

VDD

PH2

PH3

VSS VSS VSS VSS VSS

VSS VSS VSS VSS VSS

VSS

VSS

NC

VDD

PC9 PA8

PC8 PC7

H

J

PH1/O

SCOU

T

NRST

PF2 PF1 PH4

PF3 PF4 PH5

VSS VSS VSS VSS VSS

VSS VSS VSS VSS VSS

VSS

VDD

VDD

VDD

PG8 PC6

PG7 PG6

K PF7 PF6 PF5 VDD VSS VSS VSS VSS VSS PH12 PG5 PG4 PG3

L

PF10

PF9 PF8 NC

GigaDevice GD32F470Ix

BGA176

PH11 PH10 PD15

PG2

M VSSA PC0 PC1 PC2 PC3 PB2 PG1 VSS VSS NC PH6 PH8 PH9 PD14 PD13

N

VREFN

PA1 PA0-

WKUP

PA4 PC4

PF13

PG0

VDD VDD VDD PE13

PH7

PD12

PD11 PD10

P VREFP PA2 PA6 PA5 PC5 PF12 PF15 PE8 PE9 PE11 PE14 PB12 PB13 PD9 PD8

R VDDA PA3 PA7 PB1 PB0 PF11 PF14 PE7 PE10 PE12 PE15 PB10 PB11 PB14 PB15

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**Figure 2-3. GD32F470Zx LQFP144 pinouts**

144143142141140139138137136135134133132131130129128127126125124123122121120119118117116115114113112111110109

PE2 PE3 PE4 PE5 PE6

VBAT

PC13-TAMPER-RTC

PC14-OSC32IN

PC15-OSC32OUT PF0 PF1 PF2 PF3 PF4 PF5 VSS VDD PF6 PF7 PF8 PF9 PF10

PH0/OSCIN PH1/OSCOUT

NRST PC0 PC1 PC2 PC3 VDD VSSA VREFP

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32

GigaDevice GD32F470Zx

LQFP144

108 107 106 105 104 103 102 101 100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77

VDD VSS NC PA13 PA12 PA11 PA10 PA9 PA8 PC9 PC8 PC7 PC6 VDD VSS PG8 PG7 PG6 PG5 PG4 PG3 PG2 PD15 PD14 VDD VSS PD13 PD12 PD11 PD10 PD9 PD8

VDDA 33 76 PB15

PA0-WKUP PA1 PA2

34 35 36

75 74 73

PB14 PB13 PB12

37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72

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**Figure 2-4. GD32F470Vx BGA100 pinouts**

1 2 3 4 5 6 7 8 9 10 11 12

A PE3 PE1 PB8 BOOT0 PD7 PD5 PB4 PB3 PA15 PA14 PA13 PA12

B PE4 PE2 PB9 PB7 PB6 PD6 PD4 PD3 PD1 PC12 PC10 PA11

C PC13 PE5 PE0 VDD PB5 PD2 PD0 PC11 NC PA10

D PC14 PE6 VSS PA9 PA8 PC9

E PC15 VBAT NC PC8 PC7 PC6

F

PH0

VSS

GigaDevice GD32F470Vx

BGA100

VSS

VSS

G

H

PH1

PC0

VDD

NRST

PDR\_

ON

VDD VDD

PD15 PD14 PD13

J VSSA PC1 PC2 PD12 PD11 PD10

K VREFN PC3 PA2 PA5 PC4 PD9 PB11 PB15 PB14 PB13

L VREFP PA0 PA3 PA6 PC5 PB2 PE8 PE10 PE12 PB10 NC PB12

M VDDA PA1 PA4 PA7 PB0 PB1 PE7 PE9 PE11 PE13 PE14 PE15

**Figure 2-5. GD32F470Vx LQFP100 pinouts**

100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76

PE2 PE3 PE4 PE5 PE6

VBAT

PC13-TAMPER-RTC

PC14-OSC32IN PC15-OSC32OUT

VSS

VDD

PH0/OSCIN

PH1/OSCOUT

NRST PC0 PC1 PC2 PC3 VDD

VSSA

VREFP

VDDA

PA0-WKUP PA1 PA2

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

21 22 23 24 25

GigaDevice GD32F470Vx

LQFP100

75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51

VDD VSS NC PA13 PA12 PA11 PA10 PA9 PA8 PC9 PC8 PC7 PC6 PD15 PD14 PD13 PD12 PD11 PD10 PD9 PD8 PB15 PB14 PB13 PB12

26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50

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**2.4.**

**Memory map**

**Table 2-2. GD32F470xx memory map**

|  |  |  |  |
| --- | --- | --- | --- |
| **Pre-defined**  **Regions** | **Bus** | **Address** | **Peripherals** |
| External  Device | AHB | 0xC000 0000 - 0xDFFF FFFF | EXMC - SDRAM |
| 0xA000 1000 - 0xBFFF FFFF | Reserved |
| 0xA000 0000 - 0xA000 0FFF | EXMC - SWREG |
| External  RAM | 0x9000 0000 - 0x9FFF FFFF | EXMC - PC CARD |
| 0x7000 0000 - 0x8FFF FFFF | EXMC - NAND |
| 0x6000 0000 - 0x6FFF FFFF | EXMC - NOR/PSRAM/SRAM |
| Peripheral | AHB2 | 0x5006 0C00 - 0x5FFF FFFF | Reserved |
| 0x5006 0800 - 0x5006 0BFF | TRNG |
| 0x5005 0400 - 0x5006 07FF | Reserved |
| 0x5005 0000 - 0x5005 03FF | DCI |
| 0x5004 0000 - 0x5004 FFFF | Reserved |
| 0x5000 0000 - 0x5003 FFFF | USBFS |
| AHB1 | 0x4008 0000 - 0x4FFF FFFF | Reserved |
| 0x4004 0000 - 0x4007 FFFF | USBHS |
| 0x4002 BC00 - 0x4003 FFFF | Reserved |
| 0x4002 B000 - 0x4002 BBFF | IPA |
| 0x4002 A000 - 0x4002 AFFF | Reserved |
| 0x4002 8000 - 0x4002 9FFF | ENET |
| 0x4002 6800 - 0x4002 7FFF | Reserved |
| 0x4002 6400 - 0x4002 67FF | DMA1 |
| 0x4002 6000 - 0x4002 63FF | DMA0 |
| 0x4002 5000 - 0x4002 5FFF | Reserved |
| 0x4002 4000 - 0x4002 4FFF | BKP SRAM |
| 0x4002 3C00 - 0x4002 3FFF | FMC |
| 0x4002 3800 - 0x4002 3BFF | RCU |
| 0x4002 3400 - 0x4002 37FF | Reserved |
| 0x4002 3000 - 0x4002 33FF | CRC |
| 0x4002 2400 - 0x4002 2FFF | Reserved |
| 0x4002 2000 - 0x4002 23FF | GPIOI |
| 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| 0x4002 1800 - 0x4002 1BFF | GPIOG |
| 0x4002 1400 - 0x4002 17FF | GPIOF |
| 0x4002 1000 - 0x4002 13FF | GPIOE |
| 0x4002 0C00 - 0x4002 0FFF | GPIOD |
| 0x4002 0800 - 0x4002 0BFF | GPIOC |
| 0x4002 0400 - 0x4002 07FF | GPIOB |
| 0x4002 0000 - 0x4002 03FF | GPIOA |

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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Pre-defined**  **Regions** | **Bus** | **Address** | **Peripherals** |
| APB2 | 0x4001 6C00 - 0x4001 FFFF | Reserved |
| 0x4001 6800 - 0x4001 6BFF | TLI |
| 0x4001 5800 - 0x4001 67FF | Reserved |
| 0x4001 5400 - 0x4001 57FF | SPI5 |
| 0x4001 5000 - 0x4001 53FF | SPI4 |
| 0x4001 4C00 - 0x4001 4FFF | Reserved |
| 0x4001 4800 - 0x4001 4BFF | TIMER10 |
| 0x4001 4400 - 0x4001 47FF | TIMER9 |
| 0x4001 4000 - 0x4001 43FF | TIMER8 |
| 0x4001 3C00 - 0x4001 3FFF | EXTI |
| 0x4001 3800 - 0x4001 3BFF | SYSCFG |
| 0x4001 3400 - 0x4001 37FF | SPI3 |
| 0x4001 3000 - 0x4001 33FF | SPI0 |
| 0x4001 2C00 - 0x4001 2FFF | SDIO |
| 0x4001 2400 - 0x4001 2BFF | Reserved |
| 0x4001 2300 - 0x4001 23FF | ADC0(1) |
| 0x4001 2200 - 0x4001 22FF | ADC2 |
| 0x4001 2100 - 0x4001 21FF | ADC1 |
| 0x4001 2000 - 0x4001 20FF | ADC0 |
| 0x4001 1800 - 0x4001 1FFF | Reserved |
| 0x4001 1400 - 0x4001 17FF | USART5 |
| 0x4001 1000 - 0x4001 13FF | USART0 |
| 0x4001 0800 - 0x4001 0FFF | Reserved |
| 0x4001 0400 - 0x4001 07FF | TIMER7 |
| 0x4001 0000 - 0x4001 03FF | TIMER0 |
| APB1 | 0x4000 C800 - 0x4000 FFFF | Reserved |
| 0x4000 C400 - 0x4000 C7FF | IREF |
| 0x4000 8000 - 0x4000 C3FF | Reserved |
| 0x4000 7C00 - 0x4000 7FFF | UART7 |
| 0x4000 7800 - 0x4000 7BFF | UART6 |
| 0x4000 7400 - 0x4000 77FF | DAC0 |
| 0x4000 7000 - 0x4000 73FF | PMU |
| 0x4000 6C00 - 0x4000 6FFF | CTC |
| 0x4000 6800 - 0x4000 6BFF | CAN1 |
| 0x4000 6400 - 0x4000 67FF | CAN0 |
| 0x4000 6000 - 0x4000 63FF | Reserved |
| 0x4000 5C00 - 0x4000 5FFF | I2C2 |
| 0x4000 5800 - 0x4000 5BFF | I2C1 |
| 0x4000 5400 - 0x4000 57FF | I2C0 |
| 0x4000 5000 - 0x4000 53FF | UART4 |

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GD32F470xx Datasheet

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Pre-defined**  **Regions** | **Bus** | **Address** | **Peripherals** |
| 0x4000 4C00 - 0x4000 4FFF | UART3 |
| 0x4000 4800 - 0x4000 4BFF | USART2 |
| 0x4000 4400 - 0x4000 47FF | USART1 |
| 0x4000 4000 - 0x4000 43FF | I2S2\_add |
| 0x4000 3C00 - 0x4000 3FFF | SPI2/I2S2 |
| 0x4000 3800 - 0x4000 3BFF | SPI1/I2S1 |
| 0x4000 3400 - 0x4000 37FF | I2S1\_add |
| 0x4000 3000 - 0x4000 33FF | FWDGT |
| 0x4000 2C00 - 0x4000 2FFF | WWDGT |
| 0x4000 2800 - 0x4000 2BFF | RTC |
| 0x4000 2400 - 0x4000 27FF | Reserved |
| 0x4000 2000 - 0x4000 23FF | TIMER13 |
| 0x4000 1C00 - 0x4000 1FFF | TIMER12 |
| 0x4000 1800 - 0x4000 1BFF | TIMER11 |
| 0x4000 1400 - 0x4000 17FF | TIMER6 |
| 0x4000 1000 - 0x4000 13FF | TIMER5 |
| 0x4000 0C00 - 0x4000 0FFF | TIMER4 |
| 0x4000 0800 - 0x4000 0BFF | TIMER3 |
| 0x4000 0400 - 0x4000 07FF | TIMER2 |
| 0x4000 0000 - 0x4000 03FF | TIMER1 |
| SRAM | AHB | 0x200B 0000 - 0x3FFF FFFF | Reserved |
| 0x2003 0000 - 0x200A FFFF | ADDSRAM(512KB) |
| 0x2002 0000 - 0x2002 FFFF | SRAM2(64KB) |
| 0x2001 C000 - 0x2001 FFFF | SRAM1(16KB) |
| 0x2000 0000 - 0x2001 BFFF | SRAM0(112KB) |
| Code | AHB | 0x1FFF C010 - 0x1FFF FFFF | Reserved |
| 0x1FFF C000 - 0x1FFF C00F | Option bytes(Bank 0) |
| 0x1FFF 7A10 - 0x1FFF BFFF | Reserved |
| 0x1FFF 7800 - 0x1FFF 7A0F | OTP(512B) |
| 0x1FFF 0000 - 0x1FFF 77FF | Boot loader(30KB) |
| 0x1FFE C010 - 0x1FFE FFFF | Reserved |
| 0x1FFE C000 - 0x1FFE C00F | Option bytes(Bank 1) |
| 0x1001 0000 - 0x1FFE BFFF | Reserved |
| 0x1000 0000 - 0x1000 FFFF | TCMSRAM(64KB) |
| 0x0830 0000 - 0x0FFF FFFF | Reserved |
| 0x0800 0000 - 0x082F FFFF | Main Flash(3072KB) |
| 0x0000 0000 - 0x07FF FFFF | Aliased to the boot device |

**Note:**

(1) ADC\_SSTAT, ADC\_SYNCCTL, ADC\_SYNCDATA based on base address of ADC0.

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**2.5.**

**Clock tree**

**Figure 2-6. GD32F470xx clock tree**

CK\_HXTAL /2 to /31 11

32.768 KHz LXTAL OSC

32 KHz IRC32K

01

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RTCSRC[1:0]

CK\_RTC (to RTC)

CK\_FWDGT (to FWDGT)

CK\_OUT1

CKOUT1DIV ÷1,2,3,4,5

00 01 10 11

CKOUT1SEL[1:0]

CK\_SYS CK\_PLLI2SR CK\_HXTAL CK\_PLLP

AHB enable

HCLK

(to AHB bus,Cortex-

CK\_OUT0

CKOUT0DIV ÷1,2,3,4,5

00 01 10 11

CKOUT0SEL[1:0]

CK\_IRC16M CK\_LXTAL CK\_HXTAL CK\_PLLP

SCS[1:0]

APB1 Prescaler ÷1,2,4,8,16

M4,SRAM,DMA,peripherals)

CK\_CST ÷8

(to Cortex-M4 SysTick)

FCLK

(free running clock)

CK\_APB1

PCLK1

60 MHz max to APB1 peripherals

16 MHz IRC16M

4-32 MHz HXTAL

PLLSEL

CK\_IRC16M

CK\_HXTAL

CK\_PLLP

00

CK\_SYS

01 240 MHz max

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Clock

Monitor

AHB Prescaler ÷1,2...512

CK\_AHB

240 MHz max

TIMER1,2,3,4,5,6,

11,12,13

CK\_APB1 x1 x2 or x4

APB2 Prescaler ÷1,2,4,8,16

TIMER0,7,8, 9,10

CK\_APB2 x1

Peripheral enable

240 MHz max TIMERx enable

CK\_APB2

120 MHz max

Peripheral enable

240 MHz max

CK\_TIMERx

to TIMER1,2,3,4, 5,6,11,12,13

PCLK2

to APB2 peripherals

CK\_TIMERx

/PSC

0

1

CTC

x2 or x4

ADC

TIMERx enable

ADCCK[2]

to TIMER0,7, 8,9,10

VCO

xN

PLL

/P /Q /R

PLL48MSEL

48 MHz IRC48M

CK\_CTC CK48MSEL

Prescaler

÷2,4,6,8

ADC Prescaler ÷5,6,10,20

0

1

CK\_ADCX to ADC0,1,2

40 MHz max

VCO

/P

0

1

I2SSEL

1

0

CK48M

Peripheral enable

to USBFS USBHS TRNG

/Q

xN /R

PLLI2S

/P

VCO

/Q

xN /R

PLLSAI

ENET\_TX\_CLK

/2 or /20

0

1

I2S\_CKIN

/DIV

ENET\_PHY\_SEL

1

0

Peripheral enable

Peripheral enable

Peripheral enable

SDIO

CK\_I2Sx

to I2S

CK\_TLI

to TLI CK\_ENETTX to ENET TX

ENET\_RX\_CLK

1

0

EMBPHY

Peripheral enable

CK\_ENETRX

to ENET RX

USB HS PHY clock 24Mhz to 60Mhz

CK48M

0

1

Peripheral enable

CK\_USBHS\_ULPI to USBHS ULPI

**Legend:**

HXTAL: High speed crystal oscillator LXTAL: Low speed crystal oscillator IRC16M: Internal 16M RC oscillators IRC32K: Internal 32K RC oscillator IRC48M: Internal 48M RC oscillators

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**2.6.** **Pin definitions**

**2.6.1.**

**GD32F470Ix BGA176 pin definitions**

**Table 2-3. GD32F470Ix BGA176 pin definitions**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PE2 | A2 | I/O | 5VT | Default: PE2  Alternate: SPI3\_SCK, ENET\_MII\_TXD3, EXMC\_A23,  EVENTOUT |
| PE3 | A1 | I/O | 5VT | Default: PE3  Alternate: EXMC\_A19, EVENTOUT |
| PE4 | B1 | I/O | 5VT | Default: PE4  Alternate: SPI3\_NSS, EXMC\_A20, DCI\_D4, TLI\_B0,  EVENTOUT |
| PE5 | B2 | I/O | 5VT | Default: PE5  Alternate: TIMER8\_CH0, SPI3\_MISO, EXMC\_A21, DCI\_D6,  TLI\_G0, EVENTOUT |
| PE6 | B3 | I/O | 5VT | Default: PE6  Alternate: TIMER8\_CH1, SPI3\_MOSI, EXMC\_A22, DCI\_D7,  TLI\_G1, EVENTOUT |
| VBAT | C1 | P | - | Default: VBAT |
| PI8 | D2 | I/O | 5VT | Default: PI8  Alternate: EVENTOUT  Additional: RTC\_TAMP1, RTC\_TAMP0, RTC\_TS |
| PC13-  TAMPER-  RTC | D1 | I/O | 5VT | Default: PC13  Alternate: EVENTOUT  Additional: RTC\_TAMP0, RTC\_OUT, RTC\_TS |
| PC14-  OSC32IN | E1 | I/O | 5VT | Default: PC14 Alternate: EVENTOUT Additional: OSC32IN |
| PC15-  OSC32OU  T | F1 | I/O | 5VT | Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT |
| PI9 | D3 | I/O | 5VT | Default: PI9  Alternate: CAN0\_RX, EXMC\_D30, TLI\_VSYNC, EVENTOUT |
| PI10 | E3 | I/O | 5VT | Default: PI10  Alternate: ENET\_MII\_RX\_ER, EXMC\_D31, TLI\_HSYNC,  EVENTOUT |
| PI11 | E4 | I/O | 5VT | Default: PI11  Alternate: USBHS\_ULPI\_DIR, EVENTOUT |
| VSS | F2 | P | - | Default: VSS |
| VDD | F3 | P | - | Default: VDD |
| PF0 | E2 | I/O | 5VT | Default: PF0 |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Alternate: I2C1\_SDA, EXMC\_A0, EVENTOUT, CTC\_SYNC |
| PF1 | H3 | I/O | 5VT | Default: PF1  Alternate: I2C1\_SCL, EXMC\_A1, EVENTOUT |
| PF2 | H2 | I/O | 5VT | Default: PF2  Alternate: I2C1\_SMBA, EXMC\_A2, EVENTOUT |
| PF3 | J2 | I/O | 5VT | Default: PF3  Alternate: EXMC\_A3, EVENTOUT, I2C1\_TXFRAME  Additional: ADC2\_IN9 |
| PF4 | J3 | I/O | 5VT | Default: PF4  Alternate: EXMC\_A4, EVENTOUT  Additional: ADC2\_IN14 |
| PF5 | K3 | I/O | 5VT | Default: PF5  Alternate: EXMC\_A5, EVENTOUT  Additional: ADC2\_IN15 |
| VSS | G2 | P | - | Default: VSS |
| VDD | G3 | P | - | Default: VDD |
| PF6 | K2 | I/O | 5VT | Default: PF6  Alternate: TIMER9\_CH0, SPI4\_NSS, UART6\_RX, EXMC\_NIORD, EVENTOUT  Additional: ADC2\_IN4 |
| PF7 | K1 | I/O | 5VT | Default: PF7  Alternate: TIMER10\_CH0, SPI4\_SCK, UART6\_TX, EXMC\_NREG, EVENTOUT  Additional: ADC2\_IN5 |
| PF8 | L3 | I/O | 5VT | Default: PF8  Alternate: SPI4\_MISO, TIMER12\_CH0, EXMC\_NIOWR,  EVENTOUT  Additional: ADC2\_IN6 |
| PF9 | L2 | I/O | 5VT | Default: PF9  Alternate: SPI4\_MOSI, TIMER13\_CH0, EXMC\_CD,  EVENTOUT  Additional: ADC2\_IN7 |
| PF10 | L1 | I/O | 5VT | Default: PF10  Alternate: EXMC\_INTR, DCI\_D11, TLI\_DE, EVENTOUT  Additional: ADC2\_IN8 |
| PH0/OSCI  N | G1 | I/O | 5VT | Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN |
| PH1/OSCO  UT | H1 | I/O | 5VT | Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT |
| NRST | J1 | - | - | Default: NRST |
| PC0 | M2 | I/O | 5VT | Default: PC0  Alternate: USBHS\_ULPI\_STP, EXMC\_SDNWE, EVENTOUT |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Additional: ADC012\_IN10 |
| PC1 | M3 | I/O | 5VT | Default: PC1  Alternate: SPI2\_MOSI, I2S2\_SD, SPI1\_MOSI, I2S1\_SD, ENET\_MDC, EVENTOUT  Additional: ADC012\_IN11 |
| PC2 | M4 | I/O | 5VT | Default: PC2  Alternate: SPI1\_MISO, I2S1\_ADD\_SD, USBHS\_ULPI\_DIR,  ENET\_MII\_TXD2, EXMC\_SDNE0, EVENTOUT  Additional: ADC012\_IN12 |
| PC3 | M5 | I/O | 5VT | Default: PC3  Alternate: SPI1\_MOSI, I2S1\_SD, USBHS\_ULPI\_NXT, ENET\_MII\_TX\_CLK, EXMC\_SDCKE0, EVENTOUT Additional: ADC012\_IN13 |
| VSSA | M1 | P | - | Default: VSSA |
| VREFN | N1 | P | - | Default: VREFN |
| VREFP | P1 | P | - | Default: VREFP |
| VDDA | R1 | P | - | Default: VDDA |
| PA0-WKUP | N3 | I/O | 5VT | Default: PA0  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER4\_CH0, TIMER7\_ETI, USART1\_CTS, UART3\_TX, ENET\_MII\_CRS, EVENTOUT  Additional: ADC012\_IN0, WKUP |
| PA1 | N2 | I/O | 5VT | Default: PA1  Alternate: TIMER1\_CH1, TIMER4\_CH1, SPI3\_MOSI, USART1\_RTS, UART3\_RX, ENET\_MII\_RX\_CLK, ENET\_RMII\_REF\_CLK, EVENTOUT  Additional: ADC012\_IN1 |
| PA2 | P2 | I/O | 5VT | Default: PA2  Alternate: TIMER1\_CH2, TIMER4\_CH2, TIMER8\_CH0, I2S\_CKIN, USART1\_TX, ENET\_MDIO, EVENTOUT Additional: ADC012\_IN2 |
| PH2 | F4 | I/O | 5VT | Default: PH2  Alternate: ENET\_MII\_CRS, EXMC\_SDCKE0, TLI\_R0,  EVENTOUT |
| PH3 | G4 | I/O | 5VT | Default: PH3  Alternate: ENET\_MII\_COL, EXMC\_SDNE0, TLI\_R1,  EVENTOUT, I2C1\_TXFRAME |
| PH4 | H4 | I/O | 5VT | Default: PH4  Alternate: I2C1\_SCL, USBHS\_ULPI\_NXT, EVENTOUT |
| PH5 | J4 | I/O | 5VT | Default: PH5  Alternate: I2C1\_SDA, SPI4\_NSS, EXMC\_SDNWE,  EVENTOUT |
| PA3 | R2 | I/O | 5VT | Default: PA3  Alternate: TIMER1\_CH3, TIMER4\_CH3, TIMER8\_CH1, |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | I2S1\_MCK, USART1\_RX, USBHS\_ULPI\_D0, ENET\_MII\_COL, TLI\_B5, EVENTOUT Additional: ADC012\_IN3 |
| NC | L4 | - | - | - |
| VDD | K4 | P | - | Default: VDD |
| PA4 | N4 | I/O |  | Default: PA4  Alternate: SPI0\_NSS, SPI2\_NSS, I2S2\_WS, USART1\_CK, USBHS\_SOF, DCI\_HSYNC, TLI\_VSYNC, EVENTOUT Additional: ADC01\_IN4, DAC0\_OUT0 |
| PA5 | P4 | I/O |  | Default: PA5  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER7\_CH0\_ON,  SPI0\_SCK, USBHS\_ULPI\_CK, EVENTOUT  Additional: ADC01\_IN5, DAC0\_OUT1 |
| PA6 | P3 | I/O | 5VT | Default: PA6  Alternate: TIMER0\_BRKIN, TIMER2\_CH0, TIMER7\_BRKIN, SPI0\_MISO, I2S1\_MCK, TIMER12\_CH0, SDIO\_CMD, DCI\_PIXCLK, TLI\_G2, EVENTOUT  Additional: ADC01\_IN6 |
| PA7 | R3 | I/O | 5VT | Default: PA7  Alternate: TIMER0\_CH0\_ON, TIMER2\_CH1, TIMER7\_CH0\_ON, SPI0\_MOSI, TIMER13\_CH0, ENET\_MII\_RX\_DV, ENET\_RMII\_CRS\_DV, EXMC\_SDNWE, EVENTOUT  Additional: ADC01\_IN7 |
| PC4 | N5 | I/O | 5VT | Default: PC4  Alternate: ENET\_MII\_RXD0, ENET\_RMII\_RXD0, EXMC\_SDNE0, EVENTOUT  Additional: ADC01\_IN14 |
| PC5 | P5 | I/O | 5VT | Default: PC5  Alternate: USART2\_RX, ENET\_MII\_RXD1, ENET\_RMII\_RXD1, EXMC\_SDCKE0, EVENTOUT Additional: ADC01\_IN15 |
| PB0 | R5 | I/O | 5VT | Default: PB0  Alternate: TIMER0\_CH1\_ON, TIMER2\_CH2, TIMER7\_CH1\_ON, SPI4\_SCK, SPI2\_MOSI, I2S2\_SD, TLI\_R3, USBHS\_ULPI\_D1, ENET\_MII\_RXD2, SDIO\_D1, EVENTOUT  Additional: ADC01\_IN8, IREF |
| PB1 | R4 | I/O | 5VT | Default: PB1  Alternate: TIMER0\_CH2\_ON, TIMER2\_CH3, TIMER7\_CH2\_ON, SPI4\_NSS, TLI\_R6, USBHS\_ULPI\_D2, ENET\_MII\_RXD3, SDIO\_D2, EVENTOUT  Additional: ADC01\_IN9 |
| PB2 | M6 | I/O | 5VT | Default: PB2, BOOT1  Alternate: TIMER1\_CH3, SPI2\_MOSI, I2S2\_SD, |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | USBHS\_ULPI\_D4, SDIO\_CK, EVENTOUT |
| PF11 | R6 | I/O | 5VT | Default: PF11  Alternate: SPI4\_MOSI, EXMC\_SDNRAS, DCI\_D12,  EVENTOUT |
| PF12 | P6 | I/O | 5VT | Default: PF12  Alternate: EXMC\_A6, EVENTOUT |
| VSS | M8 | P | - | Default: VSS |
| VDD | N8 | P | - | Default: VDD |
| PF13 | N6 | I/O | 5VT | Default: PF13  Alternate: EXMC\_A7, EVENTOUT |
| PF14 | R7 | I/O | 5VT | Default: PF14  Alternate: EXMC\_A8, EVENTOUT |
| PF15 | P7 | I/O | 5VT | Default: PF15  Alternate: EXMC\_A9, EVENTOUT |
| PG0 | N7 | I/O | 5VT | Default: PG0  Alternate: EXMC\_A10, EVENTOUT |
| PG1 | M7 | I/O | 5VT | Default: PG1  Alternate: EXMC\_A11, EVENTOUT |
| PE7 | R8 | I/O | 5VT | Default: PE7  Alternate: TIMER0\_ETI, UART6\_RX, EXMC\_D4,  EVENTOUT |
| PE8 | P8 | I/O | 5VT | Default: PE8  Alternate: TIMER0\_CH0\_ON, UART6\_TX, EXMC\_D5,  EVENTOUT |
| PE9 | P9 | I/O | 5VT | Default: PE9  Alternate: TIMER0\_CH0, EXMC\_D6, EVENTOUT |
| VSS | M9 | P | - | Default: VSS |
| VDD | N9 | P | - | Default: VDD |
| PE10 | R9 | I/O | 5VT | Default: PE10  Alternate: TIMER0\_CH1\_ON, EXMC\_D7, EVENTOUT |
| PE11 | P10 | I/O | 5VT | Default: PE11  Alternate: TIMER0\_CH1, SPI3\_NSS, SPI4\_NSS, EXMC\_D8,  TLI\_G3, EVENTOUT |
| PE12 | R10 | I/O | 5VT | Default: PE12  Alternate: TIMER0\_CH2\_ON, SPI3\_SCK, SPI4\_SCK,  EXMC\_D9, TLI\_B4, EVENTOUT |
| PE13 | N11 | I/O | 5VT | Default: PE13  Alternate: TIMER0\_CH2, SPI3\_MISO, SPI4\_MISO,  EXMC\_D10, TLI\_DE, EVENTOUT |
| PE14 | P11 | I/O | 5VT | Default: PE14  Alternate: TIMER0\_CH3, SPI3\_MOSI, SPI4\_MOSI,  EXMC\_D11, TLI\_PIXCLK, EVENTOUT |
| PE15 | R11 | I/O | 5VT | Default: PE15  Alternate: TIMER0\_BRKIN, EXMC\_D12, TLI\_R7, |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | EVENTOUT |
| PB10 | R12 | I/O | 5VT | Default: PB10  Alternate: TIMER1\_CH2, I2C1\_SCL, SPI1\_SCK, I2S1\_CK, I2S2\_MCK, USART2\_TX, USBHS\_ULPI\_D3, ENET\_MII\_RX\_ER, SDIO\_D7, TLI\_G4, EVENTOUT |
| PB11 | R13 | I/O | 5VT | Default: PB11  Alternate: TIMER1\_CH3, I2C1\_SDA, I2S\_CKIN, USART2\_RX, USBHS\_ULPI\_D4, ENET\_MII\_TX\_EN, ENET\_RMII\_TX\_EN, TLI\_G5, EVENTOUT |
| NC | M10 | - | - | - |
| VDD | N10 | P | - | Default: VDD |
| PH6 | M11 | I/O | 5VT | Default: PH6  Alternate: I2C1\_SMBA, SPI4\_SCK, TIMER11\_CH0,  ENET\_MII\_RXD2, EXMC\_SDNE1, DCI\_D8, EVENTOUT |
| PH7 | N12 | I/O | 5VT | Default: PH7  Alternate: I2C2\_SCL, SPI4\_MISO, ENET\_MII\_RXD3,  EXMC\_SDCKE1, DCI\_D9, EVENTOUT |
| PH8 | M12 | I/O | 5VT | Default: PH8  Alternate: I2C2\_SDA, EXMC\_D16, DCI\_HSYNC, TLI\_R2,  EVENTOUT |
| PH9 | M13 | I/O | 5VT | Default: PH9  Alternate: I2C2\_SMBA, TIMER11\_CH1, EXMC\_D17,  DCI\_D0, TLI\_R3, EVENTOUT |
| PH10 | L13 | I/O | 5VT | Default: PH10  Alternate: TIMER4\_CH0, EXMC\_D18, DCI\_D1, TLI\_R4,  EVENTOUT, I2C2\_TXFRAME |
| PH11 | L12 | I/O | 5VT | Default: PH11  Alternate: TIMER4\_CH1, EXMC\_D19, DCI\_D2, TLI\_R5,  EVENTOUT |
| PH12 | K12 | I/O | 5VT | Default: PH12  Alternate: TIMER4\_CH2, EXMC\_D20, DCI\_D3, TLI\_R6,  EVENTOUT |
| VSS | H12 | P | - | Default: VSS |
| VDD | J12 | P | - | Default: VDD |
| PB12 | P12 | I/O | 5VT | Default: PB12  Alternate: TIMER0\_BRKIN, I2C1\_SMBA, SPI1\_NSS, I2S1\_WS, SPI3\_NSS, USART2\_CK, CAN1\_RX, USBHS\_ULPI\_D5, ENET\_MII\_TXD0, ENET\_RMII\_TXD0, USBHS\_ID, EVENTOUT |
| PB13 | P13 | I/O | 5VT | Default: PB13  Alternate: TIMER0\_CH0\_ON, SPI1\_SCK, I2S1\_CK, SPI3\_SCK, USART2\_CTS, CAN1\_TX, USBHS\_ULPI\_D6, ENET\_MII\_TXD1, ENET\_RMII\_TXD1, EVENTOUT, I2C1\_TXFRAME |

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GD32F470xx Datasheet

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Additional: USBHS\_VBUS |
| PB14 | R14 | I/O | 5VT | Default: PB14  Alternate: TIMER0\_CH1\_ON, TIMER7\_CH1\_ON, SPI1\_MISO, I2S1\_ADD\_SD, USART2\_RTS, TIMER11\_CH0, USBHS\_DM, EVENTOUT |
| PB15 | R15 | I/O | 5VT | Default: PB15  Alternate: RTC\_REFIN, TIMER0\_CH2\_ON, TIMER7\_CH2\_ON, SPI1\_MOSI, I2S1\_SD, TIMER11\_CH1, USBHS\_DP, EVENTOUT |
| PD8 | P15 | I/O | 5VT | Default: PD8  Alternate: USART2\_TX, EXMC\_D13, EVENTOUT |
| PD9 | P14 | I/O | 5VT | Default: PD9  Alternate: USART2\_RX, EXMC\_D14, EVENTOUT |
| PD10 | N15 | I/O | 5VT | Default: PD10  Alternate: USART2\_CK, EXMC\_D15, TLI\_B3, EVENTOUT |
| PD11 | N14 | I/O | 5VT | Default: PD11  Alternate: USART2\_CTS, EXMC\_A16/EXMC\_CLE,  EVENTOUT |
| PD12 | N13 | I/O | 5VT | Default: PD12  Alternate: TIMER3\_CH0, USART2\_RTS,  EXMC\_A17/EXMC\_ALE, EVENTOUT |
| PD13 | M15 | I/O | 5VT | Default: PD13  Alternate: TIMER3\_CH1, EXMC\_A18, EVENTOUT |
| VDD | J13 | P | - | Default: VDD |
| PD14 | M14 | I/O | 5VT | Default: PD14  Alternate: TIMER3\_CH2, EXMC\_D0, EVENTOUT |
| PD15 | L14 | I/O | 5VT | Default: PD15  Alternate: TIMER3\_CH3, EXMC\_D1, EVENTOUT,  CTC\_SYNC |
| PG2 | L15 | I/O | 5VT | Default: PG2  Alternate: EXMC\_A12, EVENTOUT |
| PG3 | K15 | I/O | 5VT | Default: PG3  Alternate: EXMC\_A13, EVENTOUT |
| PG4 | K14 | I/O | 5VT | Default: PG4  Alternate: EXMC\_A14, EVENTOUT |
| PG5 | K13 | I/O | 5VT | Default: PG5  Alternate: EXMC\_A15, EVENTOUT |
| PG6 | J15 | I/O | 5VT | Default: PG6  Alternate: EXMC\_INT1, DCI\_D12, TLI\_R7, EVENTOUT |
| PG7 | J14 | I/O | 5VT | Default: PG7  Alternate: USART5\_CK, EXMC\_INT2, DCI\_D13,  TLI\_PIXCLK, EVENTOUT |
| PG8 | H14 | I/O | 5VT | Default: PG8  Alternate: SPI5\_NSS, USART5\_RTS, ENET\_PPS\_OUT,  EXMC\_SDCLK, EVENTOUT |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| VSS | G12 | P | - | Default: VSS |
| VDD | H13 | P | - | Default: VDD |
| PC6 | H15 | I/O | 5VT | Default: PC6  Alternate: TIMER2\_CH0, TIMER7\_CH0, I2S1\_MCK,  USART5\_TX, SDIO\_D6, DCI\_D0, TLI\_HSYNC, EVENTOUT |
| PC7 | G15 | I/O | 5VT | Default: PC7  Alternate: TIMER2\_CH1, TIMER7\_CH1, SPI1\_SCK, I2S1\_CK, I2S2\_MCK, USART5\_RX, SDIO\_D7, DCI\_D1, TLI\_G6, EVENTOUT |
| PC8 | G14 | I/O | 5VT | Default: PC8  Alternate: TIMER2\_CH2, TIMER7\_CH2, USART5\_CK,  SDIO\_D0, DCI\_D2, EVENTOUT |
| PC9 | F14 | I/O | 5VT | Default: PC9  Alternate: CK\_OUT1, TIMER2\_CH3, TIMER7\_CH3,  I2C2\_SDA, I2S\_CKIN, SDIO\_D1, DCI\_D3, EVENTOUT |
| PA8 | F15 | I/O | 5VT | Default: PA8  Alternate: CK\_OUT0, TIMER0\_CH0, I2C2\_SCL, USART0\_CK, USBFS\_SOF, SDIO\_D1, TLI\_R6, EVENTOUT, CTC\_SYNC |
| PA9 | E15 | I/O | 5VT | Default: PA9  Alternate: TIMER0\_CH1, I2C2\_SMBA, SPI1\_SCK, I2S1\_CK, USART0\_TX, SDIO\_D2, DCI\_D0, EVENTOUT  Additional: USBFS\_VBUS |
| PA10 | D15 | I/O | 5VT | Default: PA10  Alternate: TIMER0\_CH2, SPI4\_MOSI, USART0\_RX,  USBFS\_ID, DCI\_D1, EVENTOUT, I2C2\_TXFRAME |
| PA11 | C15 | I/O | 5VT | Default: PA11  Alternate: TIMER0\_CH3, SPI3\_MISO, USART0\_CTS,  USART5\_TX, CAN0\_RX, USBFS\_DM, TLI\_R4, EVENTOUT |
| PA12 | B15 | I/O | 5VT | Default: PA12  Alternate: TIMER0\_ETI, SPI4\_MISO, USART0\_RTS,  USART5\_RX, CAN0\_TX, USBFS\_DP, TLI\_R5, EVENTOUT |
| PA13 | A15 | I/O | 5VT | Default: JTMS, SWDIO, PA13  Alternate: EVENTOUT |
| NC | F13 | - | - | - |
| VSS | F12 | P | - | Default: VSS |
| VDD | G13 | P | - | Default: VDD |
| PH13 | E12 | I/O | 5VT | Default: PH13  Alternate: TIMER7\_CH0\_ON, CAN0\_TX, EXMC\_D21,  TLI\_G2, EVENTOUT |
| PH14 | E13 | I/O | 5VT | Default: PH14  Alternate: TIMER7\_CH1\_ON, EXMC\_D22, DCI\_D4, TLI\_G3,  EVENTOUT |
| PH15 | D13 | I/O | 5VT | Default: PH15 |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Alternate: TIMER7\_CH2\_ON, EXMC\_D23, DCI\_D11,  TLI\_G4, EVENTOUT |
| PI0 | E14 | I/O | 5VT | Default: PI0  Alternate: TIMER4\_CH3, SPI1\_NSS, I2S1\_WS, EXMC\_D24,  DCI\_D13, TLI\_G5, EVENTOUT |
| PI1 | D14 | I/O | 5VT | Default: PI1  Alternate: SPI1\_SCK, I2S1\_CK, EXMC\_D25, DCI\_D8,  TLI\_G6, EVENTOUT |
| PI2 | C14 | I/O | 5VT | Default: PI2  Alternate: TIMER7\_CH3, SPI1\_MISO, I2S1\_ADD\_SD,  EXMC\_D26, DCI\_D9, TLI\_G7, EVENTOUT |
| PI3 | C13 | I/O | 5VT | Default: PI3  Alternate: TIMER7\_ETI, SPI1\_MOSI, I2S1\_SD, EXMC\_D27,  DCI\_D10, EVENTOUT |
| VSS | D9 | P | - | Default: VSS |
| VDD | C9 | P | - | Default: VDD |
| PA14 | A14 | I/O | 5VT | Default: JTCK, SWCLK, PA14  Alternate: EVENTOUT |
| PA15 | A13 | I/O | 5VT | Default: JTDI, PA15  Alternate: TIMER1\_CH0, TIMER1\_ETI, SPI0\_NSS,  SPI2\_NSS, I2S2\_WS, USART0\_TX, EVENTOUT |
| PC10 | B14 | I/O | 5VT | Default: PC10  Alternate: SPI2\_SCK, I2S2\_CK, USART2\_TX, UART3\_TX,  SDIO\_D2, DCI\_D8, TLI\_R2, EVENTOUT |
| PC11 | B13 | I/O | 5VT | Default: PC11  Alternate: I2S2\_ADD\_SD, SPI2\_MISO, USART2\_RX,  UART3\_RX, SDIO\_D3, DCI\_D4, EVENTOUT |
| PC12 | A12 | I/O | 5VT | Default: PC12  Alternate: I2C1\_SDA, SPI2\_MOSI, I2S2\_SD, USART2\_CK,  UART4\_TX, SDIO\_CK, DCI\_D9, EVENTOUT |
| PD0 | B12 | I/O | 5VT | Default: PD0  Alternate: SPI3\_MISO, SPI2\_MOSI, I2S2\_SD, CAN0\_RX,  EXMC\_D2, EVENTOUT |
| PD1 | C12 | I/O | 5VT | Default: PD1  Alternate: SPI1\_NSS, I2S1\_WS, CAN0\_TX, EXMC\_D3,  EVENTOUT |
| PD2 | D12 | I/O | 5VT | Default: PD2  Alternate: TIMER2\_ETI, UART4\_RX, SDIO\_CMD, DCI\_D11,  EVENTOUT |
| PD3 | D11 | I/O | 5VT | Default: PD3  Alternate: SPI1\_SCK, I2S1\_CK, USART1\_CTS, EXMC\_CLK,  DCI\_D5, TLI\_G7, EVENTOUT |
| PD4 | D10 | I/O | 5VT | Default: PD4  Alternate: USART1\_RTS, EXMC\_NOE, EVENTOUT |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PD5 | C11 | I/O | 5VT | Default: PD5  Alternate: USART1\_TX, EXMC\_NWE, EVENTOUT |
| VSS | D8 | P | - | Default: VSS |
| VDD | C8 | P | - | Default: VDD |
| PD6 | B11 | I/O | 5VT | Default: PD6  Alternate: SPI2\_MOSI, I2S2\_SD, USART1\_RX,  EXMC\_NWAIT, DCI\_D10, TLI\_B2, EVENTOUT |
| PD7 | A11 | I/O | 5VT | Default: PD7  Alternate: USART1\_CK, EXMC\_NE0, EXMC\_NCE1,  EVENTOUT |
| PG9 | C10 | I/O | 5VT | Default: PG9  Alternate: USART5\_RX, EXMC\_NE1, EXMC\_NCE2,  DCI\_VSYNC, EVENTOUT |
| PG10 | B10 | I/O | 5VT | Default: PG10  Alternate: SPI5\_IO2, TLI\_G3, EXMC\_NCE3\_0, EXMC\_NE2,  DCI\_D2, TLI\_B2, EVENTOUT |
| PG11 | B9 | I/O | 5VT | Default: PG11  Alternate: SPI5\_IO3, SPI3\_SCK, ENET\_MII\_TX\_EN, ETH\_RMII\_TX\_EN, EXMC\_NCE3\_1, DCI\_D3, TLI\_B3, EVENTOUT |
| PG12 | B8 | I/O | 5VT | Default: PG12  Alternate: SPI5\_MISO, SPI3\_MISO, USART5\_RTS, TLI\_B4,  EXMC\_NE3, TLI\_B1, EVENTOUT |
| PG13 | A8 | I/O | 5VT | Default: PG13  Alternate: SPI5\_SCK, SPI3\_MOSI, USART5\_CTS, ENET\_MII\_TXD0, ENET\_RMII\_TXD0, EXMC\_A24, EVENTOUT |
| PG14 | A7 | I/O | 5VT | Default: PG14  Alternate: SPI5\_MOSI, SPI3\_NSS, USART5\_TX, ENET\_MII\_TXD1, ENET\_RMII\_TXD1, EXMC\_A25, EVENTOUT |
| VSS | D7 | P | - | Default: VSS |
| VDD | C7 | P | - | Default: VDD |
| PG15 | B7 | I/O | 5VT | Default: PG15  Alternate: USART5\_CTS, EXMC\_SDNCAS, DCI\_D13,  EVENTOUT |
| PB3 | A10 | I/O | 5VT | Default: JTDO, PB3  Alternate: TRACESWO, TIMER1\_CH1, SPI0\_SCK,  SPI2\_SCK, I2S2\_CK, USART0\_RX, I2C1\_SDA, EVENTOUT |
| PB4 | A9 | I/O | 5VT | Default: JNTRST, PB4  Alternate: TIMER2\_CH0, SPI0\_MISO, SPI2\_MISO, I2S2\_ADD\_SD, I2C2\_SDA, SDIO\_D0, EVENTOUT, I2C0\_TXFRAME |
| PB5 | A6 | I/O | 5VT | Default: PB5 |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Ix BGA176** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Alternate: TIMER2\_CH1, I2C0\_SMBA, SPI0\_MOSI, SPI2\_MOSI, I2S2\_SD, CAN1\_RX, USBHS\_ULPI\_D7, ENET\_PPS\_OUT, EXMC\_SDCKE1, DCI\_D10, EVENTOUT |
| PB6 | B6 | I/O | 5VT | Default: PB6  Alternate: TIMER3\_CH0, I2C0\_SCL, USART0\_TX,  CAN1\_TX, EXMC\_SDNE1, DCI\_D5, EVENTOUT |
| PB7 | B5 | I/O | 5VT | Default: PB7  Alternate: TIMER3\_CH1, I2C0\_SDA, USART0\_RX,  EXMC\_NL/EXMC\_NADV, DCI\_VSYNC, EVENTOUT |
| BOOT0 | D6 | I/O | 5VT | Default: BOOT0 |
| PB8 | A5 | I/O | 5VT | Default: PB8  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER3\_CH2, TIMER9\_CH0, I2C0\_SCL, SPI4\_MOSI, CAN0\_RX, ENET\_MII\_TXD3, SDIO\_D4, DCI\_D6, TLI\_B6, EVENTOUT |
| PB9 | B4 | I/O | 5VT | Default: PB9  Alternate: TIMER1\_CH1, TIMER3\_CH3, TIMER10\_CH0, I2C0\_SDA, SPI1\_NSS, I2S1\_WS, CAN0\_TX, SDIO\_D5, DCI\_D7, TLI\_B7, EVENTOUT |
| PE0 | A4 | I/O | 5VT | Default: PE0  Alternate: TIMER3\_ETI, UART7\_RX, EXMC\_NBL0, DCI\_D2,  EVENTOUT |
| PE1 | A3 | I/O | 5VT | Default: PE1  Alternate: TIMER0\_CH1\_ON, UART7\_TX, EXMC\_NBL1,  DCI\_D3, EVENTOUT |
| VSS | D5 | P | - | Default: VSS |
| PDR\_ON | C6 | P | - | Default: PDR\_ON(3) |
| VDD | C5 | P | - | Default: VDD |
| PI4 | D4 | I/O | 5VT | Default: PI4  Alternate: TIMER7\_BRKIN, EXMC\_NBL2, DCI\_D5, TLI\_B4,  EVENTOUT |
| PI5 | C4 | I/O | 5VT | Default: PI5  Alternate: TIMER7\_CH0, EXMC\_NBL3, DCI\_VSYNC,  TLI\_B5, EVENTOUT |
| PI6 | C3 | I/O | 5VT | Default: PI6  Alternate: TIMER7\_CH1, EXMC\_D28, DCI\_D6, TLI\_B6,  EVENTOUT |
| PI7 | C2 | I/O | 5VT | Default: PI7  Alternate: TIMER7\_CH2, EXMC\_D29, DCI\_D7, TLI\_B7,  EVENTOUT |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) PDR\_ON pin·should·be·pulled-up·to·VDD, refer to [***Figure***](#PageMark84)[***4-4.***](#PageMark84)[***Recommended***](#PageMark84)[***PDR\_ON***](#PageMark84)

[***pin***](#PageMark84)[***circuit***](#PageMark84).

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**2.6.2.**

**GD32F470Zx LQFP144 pin definitions**

**Table 2-4. GD32F470Zx LQFP144 pin definitions**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PE2 | 1 | I/O | 5VT | Default: PE2  Alternate: SPI3\_SCK, ENET\_MII\_TXD3, EXMC\_A23,  EVENTOUT |
| PE3 | 2 | I/O | 5VT | Default: PE3  Alternate: EXMC\_A19, EVENTOUT |
| PE4 | 3 | I/O | 5VT | Default: PE4  Alternate: SPI3\_NSS, EXMC\_A20, DCI\_D4, TLI\_B0,  EVENTOUT |
| PE5 | 4 | I/O | 5VT | Default: PE5  Alternate: TIMER8\_CH0, SPI3\_MISO, EXMC\_A21,  DCI\_D6, TLI\_G0, EVENTOUT |
| PE6 | 5 | I/O | 5VT | Default: PE6  Alternate: TIMER8\_CH1, SPI3\_MOSI, EXMC\_A22,  DCI\_D7, TLI\_G1, EVENTOUT |
| VBAT | 6 | P | - | Default: VBAT |
| PC13-  TAMPER-  RTC | 7 | I/O | 5VT | Default: PC13 Alternate: EVENTOUT  Additional: RTC\_TAMP0, RTC\_OUT, RTC\_TS |
| PC14-  OSC32IN | 8 | I/O | 5VT | Default: PC14 Alternate: EVENTOUT Additional: OSC32IN |
| PC15-  OSC32OU  T | 9 | I/O | 5VT | Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT |
| PF0 | 10 | I/O | 5VT | Default: PF0  Alternate: I2C1\_SDA, EXMC\_A0, EVENTOUT, CTC\_SYNC |
| PF1 | 11 | I/O | 5VT | Default: PF1  Alternate: I2C1\_SCL, EXMC\_A1, EVENTOUT |
| PF2 | 12 | I/O | 5VT | Default: PF2  Alternate: I2C1\_SMBA, EXMC\_A2, EVENTOUT |
| PF3 | 13 | I/O | 5VT | Default: PF3  Alternate: EXMC\_A3, EVENTOUT, I2C1\_TXFRAME  Additional: ADC2\_IN9 |
| PF4 | 14 | I/O | 5VT | Default: PF4  Alternate: EXMC\_A4, EVENTOUT  Additional: ADC2\_IN14 |
| PF5 | 15 | I/O | 5VT | Default: PF5  Alternate: EXMC\_A5, EVENTOUT  Additional: ADC2\_IN15 |
| VSS | 16 | P | - | Default: VSS |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| VDD | 17 | P | - | Default: VDD |
| PF6 | 18 | I/O | 5VT | Default: PF6  Alternate: TIMER9\_CH0, SPI4\_NSS, UART6\_RX,  EXMC\_NIORD, EVENTOUT  Additional: ADC2\_IN4 |
| PF7 | 19 | I/O | 5VT | Default: PF7  Alternate: TIMER10\_CH0, SPI4\_SCK, UART6\_TX, EXMC\_NREG, EVENTOUT  Additional: ADC2\_IN5 |
| PF8 | 20 | I/O | 5VT | Default: PF8  Alternate: SPI4\_MISO, TIMER12\_CH0, EXMC\_NIOWR, EVENTOUT  Additional: ADC2\_IN6 |
| PF9 | 21 | I/O | 5VT | Default: PF9  Alternate: SPI4\_MOSI, TIMER13\_CH0, EXMC\_CD, EVENTOUT  Additional: ADC2\_IN7 |
| PF10 | 22 | I/O | 5VT | Default: PF10  Alternate: EXMC\_INTR, DCI\_D11, TLI\_DE, EVENTOUT  Additional: ADC2\_IN8 |
| PH0/OSCI  N | 23 | I/O | 5VT | Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN |
| PH1/OSCO  UT | 24 | I/O | 5VT | Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT |
| NRST | 25 | - | - | Default: NRST |
| PC0 | 26 | I/O | 5VT | Default: PC0  Alternate: USBHS\_ULPI\_STP, EXMC\_SDNWE,  EVENTOUT  Additional: ADC012\_IN10 |
| PC1 | 27 | I/O | 5VT | Default: PC1  Alternate: SPI2\_MOSI, I2S2\_SD, SPI1\_MOSI, I2S1\_SD, ENET\_MDC, EVENTOUT  Additional: ADC012\_IN11 |
| PC2 | 28 | I/O | 5VT | Default: PC2  Alternate: SPI1\_MISO, I2S1\_ADD\_SD, USBHS\_ULPI\_DIR, ENET\_MII\_TXD2, EXMC\_SDNE0, EVENTOUT  Additional: ADC012\_IN12 |
| PC3 | 29 | I/O | 5VT | Default: PC3  Alternate: SPI1\_MOSI, I2S1\_SD, USBHS\_ULPI\_NXT, ENET\_MII\_TX\_CLK, EXMC\_SDCKE0, EVENTOUT Additional: ADC012\_IN13 |
| VDD | 30 | P | - | Default: VDD |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| VSSA | 31 | P | - | Default: VSSA |
| VREFP | 32 | P | - | Default: VREFP |
| VDDA | 33 | P | - | Default: VDDA |
| PA0-WKUP | 34 | I/O | 5VT | Default: PA0  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER4\_CH0, TIMER7\_ETI, USART1\_CTS, UART3\_TX, ENET\_MII\_CRS, EVENTOUT  Additional: ADC012\_IN0, WKUP |
| PA1 | 35 | I/O | 5VT | Default: PA1  Alternate: TIMER1\_CH1, TIMER4\_CH1, SPI3\_MOSI, USART1\_RTS, UART3\_RX, ENET\_MII\_RX\_CLK, ENET\_RMII\_REF\_CLK, EVENTOUT  Additional: ADC012\_IN1 |
| PA2 | 36 | I/O | 5VT | Default: PA2  Alternate: TIMER1\_CH2, TIMER4\_CH2, TIMER8\_CH0, I2S\_CKIN, USART1\_TX, ENET\_MDIO, EVENTOUT Additional: ADC012\_IN2 |
| PA3 | 37 | I/O | 5VT | Default: PA3  Alternate: TIMER1\_CH3, TIMER4\_CH3, TIMER8\_CH1, I2S1\_MCK, USART1\_RX, USBHS\_ULPI\_D0, ENET\_MII\_COL, TLI\_B5, EVENTOUT  Additional: ADC012\_IN3 |
| VSS | 38 | P | - | Default: VSS |
| VDD | 39 | P | - | Default: VDD |
| PA4 | 40 | I/O |  | Default: PA4  Alternate: SPI0\_NSS, SPI2\_NSS, I2S2\_WS, USART1\_CK, USBHS\_SOF, DCI\_HSYNC, TLI\_VSYNC, EVENTOUT Additional: ADC01\_IN4, DAC0\_OUT0 |
| PA5 | 41 | I/O |  | Default: PA5  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER7\_CH0\_ON, SPI0\_SCK, USBHS\_ULPI\_CK, EVENTOUT  Additional: ADC01\_IN5, DAC0\_OUT1 |
| PA6 | 42 | I/O | 5VT | Default: PA6  Alternate: TIMER0\_BRKIN, TIMER2\_CH0, TIMER7\_BRKIN, SPI0\_MISO, I2S1\_MCK, TIMER12\_CH0, SDIO\_CMD, DCI\_PIXCLK, TLI\_G2, EVENTOUT Additional: ADC01\_IN6 |
| PA7 | 43 | I/O | 5VT | Default: PA7  Alternate: TIMER0\_CH0\_ON, TIMER2\_CH1, TIMER7\_CH0\_ON, SPI0\_MOSI, TIMER13\_CH0, ENET\_MII\_RX\_DV, ENET\_RMII\_CRS\_DV, EXMC\_SDNWE, EVENTOUT  Additional: ADC01\_IN7 |
| PC4 | 44 | I/O | 5VT | Default: PC4 |

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GD32F470xx Datasheet

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Alternate: ENET\_MII\_RXD0, ENET\_RMII\_RXD0,  EXMC\_SDNE0, EVENTOUT  Additional: ADC01\_IN14 |
| PC5 | 45 | I/O | 5VT | Default: PC5  Alternate: USART2\_RX, ENET\_MII\_RXD1, ENET\_RMII\_RXD1, EXMC\_SDCKE0, EVENTOUT Additional: ADC01\_IN15 |
| PB0 | 46 | I/O | 5VT | Default: PB0  Alternate: TIMER0\_CH1\_ON, TIMER2\_CH2, TIMER7\_CH1\_ON, SPI4\_SCK, SPI2\_MOSI, I2S2\_SD, TLI\_R3, USBHS\_ULPI\_D1, ENET\_MII\_RXD2, SDIO\_D1, EVENTOUT  Additional: ADC01\_IN8, IREF |
| PB1 | 47 | I/O | 5VT | Default: PB1  Alternate: TIMER0\_CH2\_ON, TIMER2\_CH3, TIMER7\_CH2\_ON, SPI4\_NSS, TLI\_R6, USBHS\_ULPI\_D2, ENET\_MII\_RXD3, SDIO\_D2, EVENTOUT  Additional: ADC01\_IN9 |
| PB2 | 48 | I/O | 5VT | Default: PB2, BOOT1  Alternate: TIMER1\_CH3, SPI2\_MOSI, I2S2\_SD,  USBHS\_ULPI\_D4, SDIO\_CK, EVENTOUT |
| PF11 | 49 | I/O | 5VT | Default: PF11  Alternate: SPI4\_MOSI, EXMC\_SDNRAS, DCI\_D12,  EVENTOUT |
| PF12 | 50 | I/O | 5VT | Default: PF12  Alternate: EXMC\_A6, EVENTOUT |
| VSS | 51 | P | - | Default: VSS |
| VDD | 52 | P | - | Default: VDD |
| PF13 | 53 | I/O | 5VT | Default: PF13  Alternate: EXMC\_A7, EVENTOUT |
| PF14 | 54 | I/O | 5VT | Default: PF14  Alternate: EXMC\_A8, EVENTOUT |
| PF15 | 55 | I/O | 5VT | Default: PF15  Alternate: EXMC\_A9, EVENTOUT |
| PG0 | 56 | I/O | 5VT | Default: PG0  Alternate: EXMC\_A10, EVENTOUT |
| PG1 | 57 | I/O | 5VT | Default: PG1  Alternate: EXMC\_A11, EVENTOUT |
| PE7 | 58 | I/O | 5VT | Default: PE7  Alternate: TIMER0\_ETI, UART6\_RX, EXMC\_D4,  EVENTOUT |
| PE8 | 59 | I/O | 5VT | Default: PE8  Alternate: TIMER0\_CH0\_ON, UART6\_TX, EXMC\_D5,  EVENTOUT |

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GD32F470xx Datasheet

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PE9 | 60 | I/O | 5VT | Default: PE9  Alternate: TIMER0\_CH0, EXMC\_D6, EVENTOUT |
| VSS | 61 | P | - | Default: VSS |
| VDD | 62 | P | - | Default: VDD |
| PE10 | 63 | I/O | 5VT | Default: PE10  Alternate: TIMER0\_CH1\_ON, EXMC\_D7, EVENTOUT |
| PE11 | 64 | I/O | 5VT | Default: PE11  Alternate: TIMER0\_CH1, SPI3\_NSS, SPI4\_NSS,  EXMC\_D8, TLI\_G3, EVENTOUT |
| PE12 | 65 | I/O | 5VT | Default: PE12  Alternate: TIMER0\_CH2\_ON, SPI3\_SCK, SPI4\_SCK,  EXMC\_D9, TLI\_B4, EVENTOUT |
| PE13 | 66 | I/O | 5VT | Default: PE13  Alternate: TIMER0\_CH2, SPI3\_MISO, SPI4\_MISO,  EXMC\_D10, TLI\_DE, EVENTOUT |
| PE14 | 67 | I/O | 5VT | Default: PE14  Alternate: TIMER0\_CH3, SPI3\_MOSI, SPI4\_MOSI,  EXMC\_D11, TLI\_PIXCLK, EVENTOUT |
| PE15 | 68 | I/O | 5VT | Default: PE15  Alternate: TIMER0\_BRKIN, EXMC\_D12, TLI\_R7,  EVENTOUT |
| PB10 | 69 | I/O | 5VT | Default: PB10  Alternate: TIMER1\_CH2, I2C1\_SCL, SPI1\_SCK, I2S1\_CK, I2S2\_MCK, USART2\_TX, USBHS\_ULPI\_D3, ENET\_MII\_RX\_ER, SDIO\_D7, TLI\_G4, EVENTOUT |
| PB11 | 70 | I/O | 5VT | Default: PB11  Alternate: TIMER1\_CH3, I2C1\_SDA, I2S\_CKIN, USART2\_RX, USBHS\_ULPI\_D4, ENET\_MII\_TX\_EN, ENET\_RMII\_TX\_EN, TLI\_G5, EVENTOUT |
| NC | 71 | - | - | - |
| VDD | 72 | P | - | Default: VDD |
| PB12 | 73 | I/O | 5VT | Default: PB12  Alternate: TIMER0\_BRKIN, I2C1\_SMBA, SPI1\_NSS, I2S1\_WS, SPI3\_NSS, USART2\_CK, CAN1\_RX, USBHS\_ULPI\_D5, ENET\_MII\_TXD0, ENET\_RMII\_TXD0, USBHS\_ID, EVENTOUT |
| PB13 | 74 | I/O | 5VT | Default: PB13  Alternate: TIMER0\_CH0\_ON, SPI1\_SCK, I2S1\_CK, SPI3\_SCK, USART2\_CTS, CAN1\_TX, USBHS\_ULPI\_D6, ENET\_MII\_TXD1, ENET\_RMII\_TXD1, EVENTOUT, I2C1\_TXFRAME  Additional: USBHS\_VBUS |
| PB14 | 75 | I/O | 5VT | Default: PB14  Alternate: TIMER0\_CH1\_ON, TIMER7\_CH1\_ON, |

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GD32F470xx Datasheet

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | SPI1\_MISO, I2S1\_ADD\_SD, USART2\_RTS,  TIMER11\_CH0, USBHS\_DM, EVENTOUT |
| PB15 | 76 | I/O | 5VT | Default: PB15  Alternate: RTC\_REFIN, TIMER0\_CH2\_ON, TIMER7\_CH2\_ON, SPI1\_MOSI, I2S1\_SD, TIMER11\_CH1, USBHS\_DP, EVENTOUT |
| PD8 | 77 | I/O | 5VT | Default: PD8  Alternate: USART2\_TX, EXMC\_D13, EVENTOUT |
| PD9 | 78 | I/O | 5VT | Default: PD9  Alternate: USART2\_RX, EXMC\_D14, EVENTOUT |
| PD10 | 79 | I/O | 5VT | Default: PD10  Alternate: USART2\_CK, EXMC\_D15, TLI\_B3, EVENTOUT |
| PD11 | 80 | I/O | 5VT | Default: PD11  Alternate: USART2\_CTS, EXMC\_A16/EXMC\_CLE,  EVENTOUT |
| PD12 | 81 | I/O | 5VT | Default: PD12  Alternate: TIMER3\_CH0, USART2\_RTS,  EXMC\_A17/EXMC\_ALE, EVENTOUT |
| PD13 | 82 | I/O | 5VT | Default: PD13  Alternate: TIMER3\_CH1, EXMC\_A18, EVENTOUT |
| VSS | 83 | P | - | Default: VSS |
| VDD | 84 | P | - | Default: VDD |
| PD14 | 85 | I/O | 5VT | Default: PD14  Alternate: TIMER3\_CH2, EXMC\_D0, EVENTOUT |
| PD15 | 86 | I/O | 5VT | Default: PD15  Alternate: TIMER3\_CH3, EXMC\_D1, EVENTOUT,  CTC\_SYNC |
| PG2 | 87 | I/O | 5VT | Default: PG2  Alternate: EXMC\_A12, EVENTOUT |
| PG3 | 88 | I/O | 5VT | Default: PG3  Alternate: EXMC\_A13, EVENTOUT |
| PG4 | 89 | I/O | 5VT | Default: PG4  Alternate: EXMC\_A14, EVENTOUT |
| PG5 | 90 | I/O | 5VT | Default: PG5  Alternate: EXMC\_A15, EVENTOUT |
| PG6 | 91 | I/O | 5VT | Default: PG6  Alternate: EXMC\_INT1, DCI\_D12, TLI\_R7, EVENTOUT |
| PG7 | 92 | I/O | 5VT | Default: PG7  Alternate: USART5\_CK, EXMC\_INT2, DCI\_D13,  TLI\_PIXCLK, EVENTOUT |
| PG8 | 93 | I/O | 5VT | Default: PG8  Alternate: SPI5\_NSS, USART5\_RTS, ENET\_PPS\_OUT,  EXMC\_SDCLK, EVENTOUT |
| VSS | 94 | P | - | Default: VSS |

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GD32F470xx Datasheet

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| VDD | 95 | P | - | Default: VDD |
| PC6 | 96 | I/O | 5VT | Default: PC6  Alternate: TIMER2\_CH0, TIMER7\_CH0, I2S1\_MCK, USART5\_TX, SDIO\_D6, DCI\_D0, TLI\_HSYNC, EVENTOUT |
| PC7 | 97 | I/O | 5VT | Default: PC7  Alternate: TIMER2\_CH1, TIMER7\_CH1, SPI1\_SCK, I2S1\_CK, I2S2\_MCK, USART5\_RX, SDIO\_D7, DCI\_D1, TLI\_G6, EVENTOUT |
| PC8 | 98 | I/O | 5VT | Default: PC8  Alternate: TIMER2\_CH2, TIMER7\_CH2, USART5\_CK,  SDIO\_D0, DCI\_D2, EVENTOUT |
| PC9 | 99 | I/O | 5VT | Default: PC9  Alternate: CK\_OUT1, TIMER2\_CH3, TIMER7\_CH3,  I2C2\_SDA, I2S\_CKIN, SDIO\_D1, DCI\_D3, EVENTOUT |
| PA8 | 100 | I/O | 5VT | Default: PA8  Alternate: CK\_OUT0, TIMER0\_CH0, I2C2\_SCL, USART0\_CK, USBFS\_SOF, SDIO\_D1, TLI\_R6, EVENTOUT, CTC\_SYNC |
| PA9 | 101 | I/O | 5VT | Default: PA9  Alternate: TIMER0\_CH1, I2C2\_SMBA, SPI1\_SCK, I2S1\_CK, USART0\_TX, SDIO\_D2, DCI\_D0, EVENTOUT Additional: USBFS\_VBUS |
| PA10 | 102 | I/O | 5VT | Default: PA10  Alternate: TIMER0\_CH2, SPI4\_MOSI, USART0\_RX,  USBFS\_ID, DCI\_D1, EVENTOUT, I2C2\_TXFRAME |
| PA11 | 103 | I/O | 5VT | Default: PA11  Alternate: TIMER0\_CH3, SPI3\_MISO, USART0\_CTS, USART5\_TX, CAN0\_RX, USBFS\_DM, TLI\_R4, EVENTOUT |
| PA12 | 104 | I/O | 5VT | Default: PA12  Alternate: TIMER0\_ETI, SPI4\_MISO, USART0\_RTS, USART5\_RX, CAN0\_TX, USBFS\_DP, TLI\_R5, EVENTOUT |
| PA13 | 105 | I/O | 5VT | Default: JTMS, SWDIO, PA13  Alternate: EVENTOUT |
| NC | 106 | - | - | - |
| VSS | 107 | P | - | Default: VSS |
| VDD | 108 | P | - | Default: VDD |
| PA14 | 109 | I/O | 5VT | Default: JTCK, SWCLK, PA14  Alternate: EVENTOUT |
| PA15 | 110 | I/O | 5VT | Default: JTDI, PA15  Alternate: TIMER1\_CH0, TIMER1\_ETI, SPI0\_NSS,  SPI2\_NSS, I2S2\_WS, USART0\_TX, EVENTOUT |

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GD32F470xx Datasheet

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PC10 | 111 | I/O | 5VT | Default: PC10  Alternate: SPI2\_SCK, I2S2\_CK, USART2\_TX, UART3\_TX,  SDIO\_D2, DCI\_D8, TLI\_R2, EVENTOUT |
| PC11 | 112 | I/O | 5VT | Default: PC11  Alternate: I2S2\_ADD\_SD, SPI2\_MISO, USART2\_RX,  UART3\_RX, SDIO\_D3, DCI\_D4, EVENTOUT |
| PC12 | 113 | I/O | 5VT | Default: PC12  Alternate: I2C1\_SDA, SPI2\_MOSI, I2S2\_SD, USART2\_CK,  UART4\_TX, SDIO\_CK, DCI\_D9, EVENTOUT |
| PD0 | 114 | I/O | 5VT | Default: PD0  Alternate: SPI3\_MISO, SPI2\_MOSI, I2S2\_SD, CAN0\_RX,  EXMC\_D2, EVENTOUT |
| PD1 | 115 | I/O | 5VT | Default: PD1  Alternate: SPI1\_NSS, I2S1\_WS, CAN0\_TX, EXMC\_D3,  EVENTOUT |
| PD2 | 116 | I/O | 5VT | Default: PD2  Alternate: TIMER2\_ETI, UART4\_RX, SDIO\_CMD,  DCI\_D11, EVENTOUT |
| PD3 | 117 | I/O | 5VT | Default: PD3  Alternate: SPI1\_SCK, I2S1\_CK, USART1\_CTS,  EXMC\_CLK, DCI\_D5, TLI\_G7, EVENTOUT |
| PD4 | 118 | I/O | 5VT | Default: PD4  Alternate: USART1\_RTS, EXMC\_NOE, EVENTOUT |
| PD5 | 119 | I/O | 5VT | Default: PD5  Alternate: USART1\_TX, EXMC\_NWE, EVENTOUT |
| VSS | 120 | P | - | Default: VSS |
| VDD | 121 | P | - | Default: VDD |
| PD6 | 122 | I/O | 5VT | Default: PD6  Alternate: SPI2\_MOSI, I2S2\_SD, USART1\_RX,  EXMC\_NWAIT, DCI\_D10, TLI\_B2, EVENTOUT |
| PD7 | 123 | I/O | 5VT | Default: PD7  Alternate: USART1\_CK, EXMC\_NE0, EXMC\_NCE1,  EVENTOUT |
| PG9 | 124 | I/O | 5VT | Default: PG9  Alternate: USART5\_RX, EXMC\_NE1, EXMC\_NCE2,  DCI\_VSYNC, EVENTOUT |
| PG10 | 125 | I/O | 5VT | Default: PG10  Alternate: SPI5\_IO2, TLI\_G3, EXMC\_NCE3\_0,  EXMC\_NE2, DCI\_D2, TLI\_B2, EVENTOUT |
| PG11 | 126 | I/O | 5VT | Default: PG11  Alternate: SPI5\_IO3, SPI3\_SCK, ENET\_MII\_TX\_EN, ENET\_RMII\_TX\_EN, EXMC\_NCE3\_1, DCI\_D3, TLI\_B3, EVENTOUT |
| PG12 | 127 | I/O | 5VT | Default: PG12 |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Alternate: SPI5\_MISO, SPI3\_MISO, USART5\_RTS,  TLI\_B4, EXMC\_NE3, TLI\_B1, EVENTOUT |
| PG13 | 128 | I/O | 5VT | Default: PG13  Alternate: SPI5\_SCK, SPI3\_MOSI, USART5\_CTS, ENET\_MII\_TXD0, ENET\_RMII\_TXD0, EXMC\_A24, EVENTOUT |
| PG14 | 129 | I/O | 5VT | Default: PG14  Alternate: SPI5\_MOSI, SPI3\_NSS, USART5\_TX, ENET\_MII\_TXD1, ENET\_RMII\_TXD1, EXMC\_A25, EVENTOUT |
| VSS | 130 | P | - | Default: VSS |
| VDD | 131 | P | - | Default: VDD |
| PG15 | 132 | I/O | 5VT | Default: PG15  Alternate: USART5\_CTS, EXMC\_SDNCAS, DCI\_D13,  EVENTOUT |
| PB3 | 133 | I/O | 5VT | Default: JTDO, PB3  Alternate: TRACESWO, TIMER1\_CH1, SPI0\_SCK, SPI2\_SCK, I2S2\_CK, USART0\_RX, I2C1\_SDA, EVENTOUT |
| PB4 | 134 | I/O | 5VT | Default: NJTRST, PB4  Alternate:TIMER2\_CH0, SPI0\_MISO, SPI2\_MISO, I2S2\_ADD\_SD, I2C2\_SDA, SDIO\_D0, EVENTOUT, I2C0\_TXFRAME |
| PB5 | 135 | I/O | 5VT | Default: PB5  Alternate:TIMER2\_CH1, I2C0\_SMBA, SPI0\_MOSI, SPI2\_MOSI, I2S2\_SD, CAN1\_RX, USBHS\_ULPI\_D7, ENET\_PPS\_OUT, EXMC\_SDCKE1, DCI\_D10, EVENTOUT |
| PB6 | 136 | I/O | 5VT | Default: PB6  Alternate:TIMER3\_CH0, I2C0\_SCL, USART0\_TX,  CAN1\_TX, EXMC\_SDNE1, DCI\_D5, EVENTOUT |
| PB7 | 137 | I/O | 5VT | Default: PB7  Alternate:TIMER3\_CH1, I2C0\_SDA, USART0\_RX,  EXMC\_NL/EXMC\_NADV, DCI\_VSYNC, EVENTOUT |
| BOOT0 | 138 | I/O | 5VT | Default: BOOT0 |
| PB8 | 139 | I/O | 5VT | Default: PB8  Alternate:TIMER1\_CH0, TIMER1\_ETI, TIMER3\_CH2, TIMER9\_CH0, I2C0\_SCL, SPI4\_MOSI, CAN0\_RX, ENET\_MII\_TXD3, SDIO\_D4, DCI\_D6, TLI\_B6, EVENTOUT |
| PB9 | 140 | I/O | 5VT | Default: PB9  Alternate:TIMER1\_CH1, TIMER3\_CH3, TIMER10\_CH0, I2C0\_SDA, SPI1\_NSS, I2S1\_WS, CAN0\_TX, SDIO\_D5, DCI\_D7, TLI\_B7, EVENTOUT |
| PE0 | 141 | I/O | 5VT | Default: PE0  Alternate: TIMER3\_ETI, UART7\_RX, EXMC\_NBL0, |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Zx LQFP144** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | DCI\_D2, EVENTOUT |
| PE1 | 142 | I/O | 5VT | Default: PE1  Alternate: TIMER0\_CH1\_ON, UART7\_TX, EXMC\_NBL1,  DCI\_D3, EVENTOUT |
| PDR\_ON | 143 | P | - | Default: PDR\_ON(3) |
| VDD | 144 | P | - | Default: VDD |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) PDR\_ON pin·should·be·pulled-up·to·VDD, refer to [***Figure***](#PageMark84)[***4-4.***](#PageMark84)[***Recommended***](#PageMark84)[***PDR\_ON***](#PageMark84)

[***pin***](#PageMark84)[***circuit***](#PageMark84).

**2.6.3.**

**GD32F470Vx BGA100 pin definitions**

**Table 2-5. GD32F470Vx BGA100 pin definitions**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **GD32F470Vx BGA100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PE2 | B2 | I/O | 5VT | Default: PE2  Alternate: SPI3\_SCK, ETH\_MII\_TXD3, EXMC\_A23,  EVENTOUT |
| PE3 | A1 | I/O | 5VT | Default: PE3  Alternate: EXMC\_A19, EVENTOUT |
| PE4 | B1 | I/O | 5VT | Default: PE4  Alternate: SPI3\_NSS, EXMC\_A20, DCI\_D4, TLI\_B0,  EVENTOUT |
| PE5 | C2 | I/O | 5VT | Default: PE5  Alternate: TIMER8\_CH0, SPI3\_MISO, EXMC\_A21, DCI\_D6,  TLI\_G0, EVENTOUT |
| PE6 | D2 | I/O | 5VT | Default: PE6  Alternate: TIMER8\_CH1, SPI3\_MOSI, EXMC\_A22, DCI\_D7,  TLI\_G1, EVENTOUT |
| VBAT | E2 | P | - | Default: VBAT |
| PC13-  TAMPER-  RTC | C1 | I/O | 5VT | Default: PC13 Alternate: EVENTOUT  Additional: RTC\_TAMP0, RTC\_OUT, RTC\_TS |
| PC14-  OSC32IN | D1 | I/O | 5VT | Default: PC14 Alternate: EVENTOUT Additional: OSC32IN |
| PC15-  OSC32OU  T | E1 | I/O | 5VT | Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx BGA100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| VSS | F2 | P | - | Default: VSS |
| VDD | G2 | P | - | Default: VDD |
| PH0/OSCI  N | F1 | I/O | 5VT | Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN |
| PH1/OSCO  UT | G1 | I/O | 5VT | Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT |
| NRST | H2 | - | - | Default: NRST |
| PC0 | H1 | I/O | 5VT | Default: PC0  Alternate: USBHS\_ULPI\_STP, EVENTOUT  Additional: ADC012\_IN10 |
| PC1 | J2 | I/O | 5VT | Default: PC1  Alternate: SPI2\_MOSI, I2S2\_SD, SPI1\_MOSI, I2S1\_SD, ETH\_MDC, EVENTOUT  Additional: ADC012\_IN11 |
| PC2 | J3 | I/O | 5VT | Default: PC2  Alternate: SPI1\_MISO, I2S1\_ADD\_SD, USBHS\_ULPI\_DIR, ETH\_MII\_TXD2, EVENTOUT  Additional: ADC012\_IN12 |
| PC3 | K2 | I/O | 5VT | Default: PC3  Alternate: SPI1\_MOSI, I2S1\_SD, USBHS\_ULPI\_NXT, ETH\_MII\_TX\_CLK, EXMC\_SDCKE0, EVENTOUT Additional: ADC012\_IN13 |
| VSSA | J1 | P | - | Default: VSSA |
| VREFN | K1 | P | - | Default: VREFN |
| VREFP | L1 | P | - | Default: VREFP |
| VDDA | M1 | P | - | Default: VDDA |
| PA0-WKUP | L2 | I/O | 5VT | Default: PA0  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER4\_CH0, TIMER7\_ETI, USART1\_CTS, UART3\_TX, ETH\_MII\_CRS, EVENTOUT  Additional: ADC012\_IN0, WKUP |
| PA1 | M2 | I/O | 5VT | Default: PA1  Alternate: TIMER1\_CH1, TIMER4\_CH1, SPI3\_MOSI, USART1\_RTS, UART3\_RX, ETH\_MII\_RX\_CLK, ETH\_RMII\_REF\_CLK, EVENTOUT  Additional: ADC012\_IN1 |
| PA2 | K3 | I/O | 5VT | Default: PA2  Alternate: TIMER1\_CH2, TIMER4\_CH2, TIMER8\_CH0, I2S\_CKIN, USART1\_TX, ETH\_MDIO, EVENTOUT Additional: ADC012\_IN2 |
| PA3 | L3 | I/O | 5VT | Default: PA3  Alternate: TIMER1\_CH3, TIMER4\_CH3, TIMER8\_CH1, |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx BGA100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | I2S1\_MCK, USART1\_RX, USBHS\_ULPI\_D0, ETH\_MII\_COL,  TLI\_B5, EVENTOUT  Additional: ADC012\_IN3 |
| NC | E3 | - | - | - |
| PA4 | M3 | I/O | TTa | Default: PA4  Alternate: SPI0\_NSS, SPI2\_NSS, I2S2\_WS, USART1\_CK, USBHS\_SOF, DCI\_HSYNC, TLI\_VSYNC, EVENTOUT Additional: ADC01\_IN4, DAC0\_OUT0 |
| PA5 | K4 | I/O | TTa | Default: PA5  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER7\_CH0\_ON,  SPI0\_SCK, USBHS\_ULPI\_CK, EVENTOUT  Additional: ADC01\_IN5, DAC0\_OUT1 |
| PA6 | L4 | I/O | 5VT | Default: PA6  Alternate: TIMER0\_BRKIN, TIMER2\_CH0, TIMER7\_BRKIN, SPI0\_MISO, I2S1\_MCK, TIMER12\_CH0, SDIO\_CMD, DCI\_PIXCLK, TLI\_G2, EVENTOUT  Additional: ADC01\_IN6 |
| PA7 | M4 | I/O | 5VT | Default: PA7  Alternate: TIMER0\_CH0\_ON, TIMER2\_CH1, TIMER7\_CH0\_ON, SPI0\_MOSI, TIMER13\_CH0, ETH\_MII\_RX\_DV, ETH\_RMII\_CRS\_DV, EVENTOUT Additional: ADC01\_IN7 |
| PC4 | K5 | I/O | 5VT | Default: PC4  Alternate: ETH\_MII\_RXD0, ETH\_RMII\_RXD0, EVENTOUT  Additional: ADC01\_IN14 |
| PC5 | L5 | I/O | 5VT | Default: PC5  Alternate: USART2\_RX, ETH\_MII\_RXD1, ETH\_RMII\_RXD1,  EXMC\_SDCKE0, EVENTOUT  Additional: ADC01\_IN15 |
| PB0 | M5 | I/O | 5VT | Default: PB0  Alternate: TIMER0\_CH1\_ON, TIMER2\_CH2, TIMER7\_CH1\_ON, SPI4\_SCK, SPI2\_MOSI, I2S2\_SD, TLI\_R3, USBHS\_ULPI\_D1, ETH\_MII\_RXD2, SDIO\_D1, EVENTOUT  Additional: ADC01\_IN8, IREF |
| PB1 | M6 | I/O | 5VT | Default: PB1  Alternate: TIMER0\_CH2\_ON, TIMER2\_CH3, TIMER7\_CH2\_ON, SPI4\_NSS, TLI\_R6, USBHS\_ULPI\_D2, ETH\_MII\_RXD3, SDIO\_D2, EVENTOUT  Additional: ADC01\_IN9 |
| PB2 | L6 | I/O | 5VT | Default: PB2, BOOT1  Alternate:TIMER1\_CH3, SPI2\_MOSI, I2S2\_SD,  USBHS\_ULPI\_D4, SDIO\_CK, EVENTOUT |
| PE7 | M7 | I/O | 5VT | Default: PE7  Alternate: TIMER0\_ETI, UART6\_RX, EXMC\_D4, |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx BGA100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | EVENTOUT |
| PE8 | L7 | I/O | 5VT | Default: PE8  Alternate: TIMER0\_CH0\_ON, UART6\_TX, EXMC\_D5,  EVENTOUT |
| PE9 | M8 | I/O | 5VT | Default: PE9  Alternate: TIMER0\_CH0, EXMC\_D6, EVENTOUT |
| PE10 | L8 | I/O | 5VT | Default: PE10  Alternate: TIMER0\_CH1\_ON, EXMC\_D7, EVENTOUT |
| PE11 | M9 | I/O | 5VT | Default: PE11  Alternate:TIMER0\_CH1, SPI3\_NSS, SPI4\_NSS, TLI\_G3,  EVENTOUT |
| PE12 | L9 | I/O | 5VT | Default: PE12  Alternate:TIMER0\_CH2\_ON, SPI3\_SCK, SPI4\_SCK, TLI\_B4,  EVENTOUT |
| PE13 | M10 | I/O | 5VT | Default: PE13  Alternate:TIMER0\_CH2, SPI3\_MISO, SPI4\_MISO, TLI\_DE,  EVENTOUT |
| PE14 | M11 | I/O | 5VT | Default: PE14  Alternate:TIMER0\_CH3, SPI3\_MOSI, SPI4\_MOSI,  TLI\_PIXCLK, EVENTOUT |
| PE15 | M12 | I/O | 5VT | Default: PE15  Alternate: TIMER0\_BRKIN, TLI\_R7, EVENTOUT |
| PB10 | L10 | I/O | 5VT | Default: PB10  Alternate:TIMER1\_CH2, I2C1\_SCL, SPI1\_SCK, I2S1\_CK, I2S2\_MCK, USART2\_TX, USBHS\_ULPI\_D3, ETH\_MII\_RX\_ER, SDIO\_D7, TLI\_G4, EVENTOUT |
| PB11 | K9 | I/O | 5VT | Default: PB11  Alternate:TIMER1\_CH3, I2C1\_SDA, I2S\_CKIN, USART2\_RX, USBHS\_ULPI\_D4, ETH\_MII\_TX\_EN, ETH\_RMII\_TX\_EN, TLI\_G5, EVENTOUT |
| NC | L11 | P | - | - |
| VSS | F12 | P | - | Default: VSS |
| VDD | G12 | P | - | Default: VDD |
| PB12 | L12 | I/O | 5VT | Default: PB12  Alternate:TIMER0\_BRKIN, I2C1\_SMBA, SPI1\_NSS, I2S1\_WS, SPI3\_NSS, USART2\_CK, CAN1\_RX, USBHS\_ULPI\_D5, ETH\_MII\_TXD0, ETH\_RMII\_TXD0, USBHS\_ID, EVENTOUT |
| PB13 | K12 | I/O | 5VT | Default: PB13  Alternate: TIMER0\_CH0\_ON, SPI1\_SCK, I2S1\_CK, SPI3\_SCK, USART2\_CTS, CAN1\_TX, USBHS\_ULPI\_D6, ETH\_MII\_TXD1, ETH\_RMII\_TXD1, EVENTOUT, I2C1\_TXFRAME  Additional: USBHS\_VBUS |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx BGA100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PB14 | K11 | I/O | 5VT | Default: PB14  Alternate:TIMER0\_CH1\_ON, TIMER7\_CH1\_ON, SPI1\_MISO, I2S1\_ADD\_SD, USART2\_RTS, TIMER11\_CH0, USBHS\_DM, EVENTOUT |
| PB15 | K10 | I/O | 5VT | Default: PB15  Alternate: RTC\_REFIN, TIMER0\_CH2\_ON, TIMER7\_CH2\_ON, SPI1\_MOSI, I2S1\_SD, TIMER11\_CH1, USBHS\_DP, EVENTOUT |
| PD9 | K8 | I/O | 5VT | Default: PD9  Alternate: USART2\_RX, EVENTOUT |
| PD10 | J12 | I/O | 5VT | Default: PD10  Alternate: USART2\_CK, TLI\_B3, EVENTOUT |
| PD11 | J11 | I/O | 5VT | Default: PD11  Alternate: USART2\_CTS, EXMC\_A16/EXMC\_CLE,  EVENTOUT |
| PD12 | J10 | I/O | 5VT | Default: PD12  Alternate: TIMER3\_CH0, USART2\_RTS,  EXMC\_A17/EXMC\_ALE, EVENTOUT |
| PD13 | H12 | I/O | 5VT | Default: PD13  Alternate: TIMER3\_CH1, EXMC\_A18, EVENTOUT |
| PD14 | H11 | I/O | 5VT | Default: PD14  Alternate: TIMER3\_CH2, EXMC\_D0, EVENTOUT |
| PD15 | H10 | I/O | 5VT | Default: PD15  Alternate: TIMER3\_CH3, EXMC\_D1, EVENTOUT,  CTC\_SYNC |
| PC6 | E12 | I/O | 5VT | Default: PC6  Alternate:TIMER2\_CH0, TIMER7\_CH0, I2S1\_MCK,  USART5\_TX, SDIO\_D6, DCI\_D0, TLI\_HSYNC, EVENTOUT |
| PC7 | E11 | I/O | 5VT | Default: PC7  Alternate:TIMER2\_CH1, TIMER7\_CH1, SPI1\_SCK, I2S1\_CK, I2S2\_MCK, USART5\_RX, SDIO\_D7, DCI\_D1, TLI\_G6, EVENTOUT |
| PC8 | E10 | I/O | 5VT | Default: PC8  Alternate: TIMER2\_CH2, TIMER7\_CH2, USART5\_CK,  SDIO\_D0, DCI\_D2, EVENTOUT |
| PC9 | D12 | I/O | 5VT | Default: PC9  Alternate:CK\_OUT1, TIMER2\_CH3, TIMER7\_CH3,  I2C2\_SDA, I2S\_CKIN, SDIO\_D1, DCI\_D3, EVENTOUT |
| PA8 | D11 | I/O | 5VT | Default: PA8  Alternate: CK\_OUT0, TIMER0\_CH0, I2C2\_SCL, USART0\_CK, USBFS\_SOF, SDIO\_D1, TLI\_R6, EVENTOUT, CTC\_SYNC |
| PA9 | D10 | I/O | 5VT | Default: PA9  Alternate: TIMER0\_CH1, I2C2\_SMBA, SPI1\_SCK, I2S1\_CK,  USART0\_TX, SDIO\_D2, DCI\_D0, EVENTOUT |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx BGA100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Additional: USBFS\_VBUS |
| PA10 | C12 | I/O | 5VT | Default: PA10  Alternate:TIMER0\_CH2, SPI4\_MOSI, USART0\_RX,  USBFS\_ID, DCI\_D1, EVENTOUT, I2C2\_TXFRAME |
| PA11 | B12 | I/O | 5VT | Default: PA11  Alternate:TIMER0\_CH3, SPI3\_MISO, USART0\_CTS,  USART5\_TX, CAN0\_RX, USBFS\_DM, TLI\_R4, EVENTOUT |
| PA12 | A12 | I/O | 5VT | Default: PA12  Alternate:TIMER0\_ETI, SPI4\_MISO, USART0\_RTS,  USART5\_RX, CAN0\_TX, USBFS\_DP, TLI\_R5, EVENTOUT |
| PA13 | A11 | I/O | 5VT | Default: JTMS, SWDIO, PA13  Alternate: EVENTOUT |
| NC | C11 | - | - | - |
| VSS | F11 | P | - | Default: VSS |
| VDD | G11 | P | - | Default: VDD |
| PA14 | A10 | I/O | 5VT | Default: JTCK, SWCLK, PA14  Alternate: EVENTOUT |
| PA15 | A9 | I/O | 5VT | Default: JTDI, PA15  Alternate:TIMER1\_CH0, TIMER1\_ETI, SPI0\_NSS,  SPI2\_NSS, I2S2\_WS, USART0\_TX, EVENTOUT |
| PC10 | B11 | I/O | 5VT | Default: PC10  Alternate:SPI2\_SCK, I2S2\_CK, USART2\_TX, UART3\_TX,  SDIO\_D2, DCI\_D8, TLI\_R2, EVENTOUT |
| PC11 | C10 | I/O | 5VT | Default: PC11  Alternate:I2S2\_ADD\_SD, SPI2\_MISO, USART2\_RX,  UART3\_RX, SDIO\_D3, DCI\_D4, EVENTOUT |
| PC12 | B10 | I/O | 5VT | Default: PC12  Alternate:I2C1\_SDA, SPI2\_MOSI, I2S2\_SD, USART2\_CK,  UART4\_TX, SDIO\_CK, DCI\_D9, EVENTOUT |
| PD0 | C9 | I/O | 5VT | Default: PD0  Alternate:SPI3\_MISO, SPI2\_MOSI, I2S2\_SD, CAN0\_RX,  EXMC\_D2, EVENTOUT |
| PD1 | B9 | I/O | 5VT | Default: PD1  Alternate: SPI1\_NSS, I2S1\_WS, CAN0\_TX, EXMC\_D3,  EVENTOUT |
| PD2 | C8 | I/O | 5VT | Default: PD2  Alternate: TIMER2\_ETI, UART4\_RX, SDIO\_CMD, DCI\_D11,  EVENTOUT |
| PD3 | B8 | I/O | 5VT | Default: PD3  Alternate: SPI1\_SCK, I2S1\_CK, USART1\_CTS, EXMC\_CLK,  DCI\_D5, TLI\_G7, EVENTOUT |
| PD4 | B7 | I/O | 5VT | Default: PD4  Alternate: USART1\_RTS, EXMC\_NOE, EVENTOUT |
| PD5 | A6 | I/O | 5VT | Default: PD5 |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx BGA100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Alternate: USART1\_TX, EXMC\_NWE, EVENTOUT |
| PD6 | B6 | I/O | 5VT | Default: PD6  Alternate:SPI2\_MOSI, I2S2\_SD, USART1\_RX,  EXMC\_NWAIT, DCI\_D10, TLI\_B2, EVENTOUT |
| PD7 | A5 | I/O | 5VT | Default: PD7  Alternate: USART1\_CK, EXMC\_NE0, EXMC\_NCE1,  EVENTOUT |
| PB3 | A8 | I/O | 5VT | Default: JTDO, PB3  Alternate: TRACESWO, TIMER1\_CH1, SPI0\_SCK,  SPI2\_SCK, I2S2\_CK, USART0\_RX, I2C1\_SDA, EVENTOUT |
| PB4 | A7 | I/O | 5VT | Default: JNTRST, PB4  Alternate:TIMER2\_CH0, SPI0\_MISO, SPI2\_MISO, I2S2\_ADD\_SD, I2C2\_SDA, SDIO\_D0, EVENTOUT, I2C0\_TXFRAME |
| PB5 | C5 | I/O | 5VT | Default: PB5  Alternate:TIMER2\_CH1, I2C0\_SMBA, SPI0\_MOSI, SPI2\_MOSI, I2S2\_SD, CAN1\_RX, USBHS\_ULPI\_D7, ETH\_PPS\_OUT, EXMC\_SDCKE1, DCI\_D10, EVENTOUT |
| PB6 | B5 | I/O | 5VT | Default: PB6  Alternate:TIMER3\_CH0, I2C0\_SCL, USART0\_TX,  CAN1\_TX, DCI\_D5, EVENTOUT |
| PB7 | B4 | I/O | 5VT | Default: PB7  Alternate:TIMER3\_CH1, I2C0\_SDA, USART0\_RX,  EXMC\_NL/EXMC\_NADV, DCI\_VSYNC, EVENTOUT |
| BOOT0 | A4 | I/O | 5VT | Default: BOOT0 |
| PB8 | A3 | I/O | 5VT | Default: PB8  Alternate:TIMER1\_CH0, TIMER1\_ETI, TIMER3\_CH2, TIMER9\_CH0, I2C0\_SCL, SPI4\_MOSI, CAN0\_RX, ETH\_MII\_TXD3, SDIO\_D4, DCI\_D6, TLI\_B6, EVENTOUT |
| PB9 | B3 | I/O | 5VT | Default: PB9  Alternate:TIMER1\_CH1, TIMER3\_CH3, TIMER10\_CH0, I2C0\_SDA, SPI1\_NSS, I2S1\_WS, CAN0\_TX, SDIO\_D5, DCI\_D7, TLI\_B7, EVENTOUT |
| PE0 | C3 | I/O | 5VT | Default: PE0  Alternate: TIMER3\_ETI, UART7\_RX, EXMC\_NBL0, DCI\_D2,  EVENTOUT |
| PE1 | A2 | I/O | 5VT | Default: PE1  Alternate: TIMER0\_CH1\_ON, UART7\_TX, EXMC\_NBL1,  DCI\_D3, EVENTOUT |
| VSS | D3 | P | - | Default: VSS |
| PDR\_ON | H3 | P | - | Default: PDR\_ON(3) |
| VDD | C4 | P | - | Default: VDD |

**Notes:**

(1) Type: I = input, O = output, P = power.

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(2) I/O Level: 5VT = 5 V tolerant.

(3) PDR\_ON pin·should·be·pulled-up·to·VDD, refer to [***Figure***](#PageMark84)[***4-4.***](#PageMark84)[***Recommended***](#PageMark84)[***PDR\_ON***](#PageMark84)

[***pin***](#PageMark84)[***circuit***](#PageMark84).

**2.6.4.**

**GD32F470Vx LQFP100 pin definitions**

**Table 2-6. GD32F470Vx LQFP100 pin definitions**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **GD32F470Vx LQFP100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PE2 | 1 | I/O | 5VT | Default: PE2  Alternate: SPI3\_SCK, ENET\_MII\_TXD3, EXMC\_A23,  EVENTOUT |
| PE3 | 2 | I/O | 5VT | Default: PE3  Alternate: EXMC\_A19, EVENTOUT |
| PE4 | 3 | I/O | 5VT | Default: PE4  Alternate: SPI3\_NSS, EXMC\_A20, DCI\_D4, TLI\_B0,  EVENTOUT |
| PE5 | 4 | I/O | 5VT | Default: PE5  Alternate: TIMER8\_CH0, SPI3\_MISO, EXMC\_A21,  DCI\_D6, TLI\_G0, EVENTOUT |
| PE6 | 5 | I/O | 5VT | Default: PE6  Alternate: TIMER8\_CH1, SPI3\_MOSI, EXMC\_A22,  DCI\_D7, TLI\_G1, EVENTOUT |
| VBAT | 6 | P | - | Default: VBAT |
| PC13-  TAMPER-  RTC | 7 | I/O | 5VT | Default: PC13 Alternate: EVENTOUT  Additional: RTC\_TAMP0, RTC\_OUT, RTC\_TS |
| PC14-  OSC32IN | 8 | I/O | 5VT | Default: PC14 Alternate: EVENTOUT Additional: OSC32IN |
| PC15-  OSC32OU  T | 9 | I/O | 5VT | Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT |
| VSS | 10 | P | - | Default: VSS |
| VDD | 11 | P | - | Default: VDD |
| PH0/OSCI  N | 12 | I/O | 5VT | Default: PH0, OSCIN Alternate: EVENTOUT Additional: OSCIN |
| PH1/OSC  OUT | 13 | I/O | 5VT | Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT |
| NRST | 14 | - | - | Default: NRST |
| PC0 | 15 | I/O | 5VT | Default: PC0  Alternate: USBHS\_ULPI\_STP, EVENTOUT  Additional: ADC012\_IN10 |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx LQFP100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PC1 | 16 | I/O | 5VT | Default: PC1  Alternate: SPI2\_MOSI, I2S2\_SD, SPI1\_MOSI, I2S1\_SD, ENET\_MDC, EVENTOUT  Additional: ADC012\_IN11 |
| PC2 | 17 | I/O | 5VT | Default: PC2  Alternate: SPI1\_MISO, I2S1\_ADD\_SD, USBHS\_ULPI\_DIR, ENET\_MII\_TXD2, EVENTOUT  Additional: ADC012\_IN12 |
| PC3 | 18 | I/O | 5VT | Default: PC3  Alternate: SPI1\_MOSI, I2S1\_SD, USBHS\_ULPI\_NXT, ENET\_MII\_TX\_CLK, EVENTOUT  Additional: ADC012\_IN13 |
| VDD | 19 | P | - | Default: VDD |
| VSSA | 20 | P | - | Default: VSSA |
| VREFP | 21 | P | - | Default: VREFP |
| VDDA | 22 | P | - | Default: VDDA |
| PA0-  WKUP | 23 | I/O | 5VT | Default: PA0  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER4\_CH0, TIMER7\_ETI, USART1\_CTS, UART3\_TX, ENET\_MII\_CRS, EVENTOUT  Additional: ADC012\_IN0, WKUP |
| PA1 | 24 | I/O | 5VT | Default: PA1  Alternate: TIMER1\_CH1, TIMER4\_CH1, SPI3\_MOSI, USART1\_RTS, UART3\_RX, ENET\_MII\_RX\_CLK, ENET\_RMII\_REF\_CLK, EVENTOUT  Additional: ADC012\_IN1 |
| PA2 | 25 | I/O | 5VT | Default: PA2  Alternate: TIMER1\_CH2, TIMER4\_CH2, TIMER8\_CH0, I2S\_CKIN, USART1\_TX, ENET\_MDIO, EVENTOUT Additional: ADC012\_IN2 |
| PA3 | 26 | I/O | 5VT | Default: PA3  Alternate: TIMER1\_CH3, TIMER4\_CH3, TIMER8\_CH1, I2S1\_MCK, USART1\_RX, USBHS\_ULPI\_D0, ENET\_MII\_COL, TLI\_B5, EVENTOUT  Additional: ADC012\_IN3 |
| VSS | 27 | P | - | Default: VSS |
| VDD | 28 | P | - | Default: VDD |
| PA4 | 29 | I/O |  | Default: PA4  Alternate: SPI0\_NSS, SPI2\_NSS, I2S2\_WS, USART1\_CK, USBHS\_SOF, DCI\_HSYNC, TLI\_VSYNC, EVENTOUT Additional: ADC01\_IN4, DAC0\_OUT0 |
| PA5 | 30 | I/O |  | Default: PA5  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER7\_CH0\_ON,  SPI0\_SCK, USBHS\_ULPI\_CK, EVENTOUT |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx LQFP100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Additional: ADC01\_IN5, DAC0\_OUT1 |
| PA6 | 31 | I/O | 5VT | Default: PA6  Alternate: TIMER0\_BRKIN, TIMER2\_CH0, TIMER7\_BRKIN, SPI0\_MISO, I2S1\_MCK, TIMER12\_CH0, SDIO\_CMD, DCI\_PIXCLK, TLI\_G2, EVENTOUT Additional: ADC01\_IN6 |
| PA7 | 32 | I/O | 5VT | Default: PA7  Alternate: TIMER0\_CH0\_ON, TIMER2\_CH1, TIMER7\_CH0\_ON, SPI0\_MOSI, TIMER13\_CH0, ENET\_MII\_RX\_DV, ENET\_RMII\_CRS\_DV, EVENTOUT Additional: ADC01\_IN7 |
| PC4 | 33 | I/O | 5VT | Default: PC4  Alternate: ENET\_MII\_RXD0, ENET\_RMII\_RXD0, EVENTOUT  Additional: ADC01\_IN14 |
| PC5 | 34 | I/O | 5VT | Default: PC5  Alternate: USART2\_RX, ENET\_MII\_RXD1, ENET\_RMII\_RXD1, EVENTOUT Additional: ADC01\_IN15 |
| PB0 | 35 | I/O | 5VT | Default: PB0  Alternate: TIMER0\_CH1\_ON, TIMER2\_CH2, TIMER7\_CH1\_ON, SPI4\_SCK, SPI2\_MOSI, I2S2\_SD, TLI\_R3, USBHS\_ULPI\_D1, ENET\_MII\_RXD2, SDIO\_D1, EVENTOUT  Additional: ADC01\_IN8, IREF |
| PB1 | 36 | I/O | 5VT | Default: PB1  Alternate: TIMER0\_CH2\_ON, TIMER2\_CH3, TIMER7\_CH2\_ON, SPI4\_NSS, TLI\_R6, USBHS\_ULPI\_D2, ENET\_MII\_RXD3, SDIO\_D2, EVENTOUT  Additional: ADC01\_IN9 |
| PB2 | 37 | I/O | 5VT | Default: PB2, BOOT1  Alternate: TIMER1\_CH3, SPI2\_MOSI, I2S2\_SD,  USBHS\_ULPI\_D4, SDIO\_CK, EVENTOUT |
| PE7 | 38 | I/O | 5VT | Default: PE7  Alternate: TIMER0\_ETI, UART6\_RX, EXMC\_D4,  EVENTOUT |
| PE8 | 39 | I/O | 5VT | Default: PE8  Alternate: TIMER0\_CH0\_ON, UART6\_TX, EXMC\_D5,  EVENTOUT |
| PE9 | 40 | I/O | 5VT | Default: PE9  Alternate: TIMER0\_CH0, EXMC\_D6, EVENTOUT |
| PE10 | 41 | I/O | 5VT | Default: PE10  Alternate: TIMER0\_CH1\_ON, EXMC\_D7, EVENTOUT |
| PE11 | 42 | I/O | 5VT | Default: PE11  Alternate: TIMER0\_CH1, SPI3\_NSS, SPI4\_NSS, |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx LQFP100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | EXMC\_D8, TLI\_G3, EVENTOUT |
| PE12 | 43 | I/O | 5VT | Default: PE12  Alternate: TIMER0\_CH2\_ON, SPI3\_SCK, SPI4\_SCK,  EXMC\_D9, TLI\_B4, EVENTOUT |
| PE13 | 44 | I/O | 5VT | Default: PE13  Alternate: TIMER0\_CH2, SPI3\_MISO, SPI4\_MISO,  EXMC\_D10, TLI\_DE, EVENTOUT |
| PE14 | 45 | I/O | 5VT | Default: PE14  Alternate: TIMER0\_CH3, SPI3\_MOSI, SPI4\_MOSI,  EXMC\_D11, TLI\_PIXCLK, EVENTOUT |
| PE15 | 46 | I/O | 5VT | Default: PE15  Alternate: TIMER0\_BRKIN, EXMC\_D12, TLI\_R7,  EVENTOUT |
| PB10 | 47 | I/O | 5VT | Default: PB10  Alternate: TIMER1\_CH2, I2C1\_SCL, SPI1\_SCK, I2S1\_CK, I2S2\_MCK, USART2\_TX, USBHS\_ULPI\_D3, ENET\_MII\_RX\_ER, SDIO\_D7, TLI\_G4, EVENTOUT |
| PB11 | 48 | I/O | 5VT | Default: PB11  Alternate: TIMER1\_CH3, I2C1\_SDA, I2S\_CKIN, USART2\_RX, USBHS\_ULPI\_D4, ENET\_MII\_TX\_EN, ENET\_RMII\_TX\_EN, TLI\_G5, EVENTOUT |
| NC | 49 | - | - | - |
| VDD | 50 | P | - | Default: VDD |
| PB12 | 51 | I/O | 5VT | Default: PB12  Alternate: TIMER0\_BRKIN, I2C1\_SMBA, SPI1\_NSS, I2S1\_WS, SPI3\_NSS, USART2\_CK, CAN1\_RX, USBHS\_ULPI\_D5, ENET\_MII\_TXD0, ENET\_RMII\_TXD0, USBHS\_ID, EVENTOUT |
| PB13 | 52 | I/O | 5VT | Default: PB13  Alternate: TIMER0\_CH0\_ON, SPI1\_SCK, I2S1\_CK, SPI3\_SCK, USART2\_CTS, CAN1\_TX, USBHS\_ULPI\_D6, ENET\_MII\_TXD1, ENET\_RMII\_TXD1, EVENTOUT, I2C1\_TXFRAME  Additional: USBHS\_VBUS |
| PB14 | 53 | I/O | 5VT | Default: PB14  Alternate: TIMER0\_CH1\_ON, TIMER7\_CH1\_ON, SPI1\_MISO, I2S1\_ADD\_SD, USART2\_RTS, TIMER11\_CH0, USBHS\_DM, EVENTOUT |
| PB15 | 54 | I/O | 5VT | Default: PB15  Alternate: RTC\_REFIN, TIMER0\_CH2\_ON, TIMER7\_CH2\_ON, SPI1\_MOSI, I2S1\_SD, TIMER11\_CH1, USBHS\_DP, EVENTOUT |
| PD8 | 55 | I/O | 5VT | Default: PD8  Alternate: USART2\_TX, EXMC\_D13, EVENTOUT |
| PD9 | 56 | I/O | 5VT | Default: PD9 |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx LQFP100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | Alternate: USART2\_RX, EXMC\_D14, EVENTOUT |
| PD10 | 57 | I/O | 5VT | Default: PD10  Alternate: USART2\_CK, EXMC\_D15, TLI\_B3, EVENTOUT |
| PD11 | 58 | I/O | 5VT | Default: PD11  Alternate: USART2\_CTS, EXMC\_A16/EXMC\_CLE,  EVENTOUT |
| PD12 | 59 | I/O | 5VT | Default: PD12  Alternate: TIMER3\_CH0, USART2\_RTS,  EXMC\_A17/EXMC\_ALE, EVENTOUT |
| PD13 | 60 | I/O | 5VT | Default: PD13  Alternate: TIMER3\_CH1, EXMC\_A18, EVENTOUT |
| PD14 | 61 | I/O | 5VT | Default: PD14  Alternate: TIMER3\_CH2, EXMC\_D0, EVENTOUT |
| PD15 | 62 | I/O | 5VT | Default: PD15  Alternate: TIMER3\_CH3, EXMC\_D1, EVENTOUT,  CTC\_SYNC |
| PC6 | 63 | I/O | 5VT | Default: PC6  Alternate: TIMER2\_CH0, TIMER7\_CH0, I2S1\_MCK, USART5\_TX, SDIO\_D6, DCI\_D0, TLI\_HSYNC, EVENTOUT |
| PC7 | 64 | I/O | 5VT | Default: PC7  Alternate: TIMER2\_CH1, TIMER7\_CH1, SPI1\_SCK, I2S1\_CK, I2S2\_MCK, USART5\_RX, SDIO\_D7, DCI\_D1, TLI\_G6, EVENTOUT |
| PC8 | 65 | I/O | 5VT | Default: PC8  Alternate: TIMER2\_CH2, TIMER7\_CH2, USART5\_CK,  SDIO\_D0, DCI\_D2, EVENTOUT |
| PC9 | 66 | I/O | 5VT | Default: PC9  Alternate: CK\_OUT1, TIMER2\_CH3, TIMER7\_CH3,  I2C2\_SDA, I2S\_CKIN, SDIO\_D1, DCI\_D3, EVENTOUT |
| PA8 | 67 | I/O | 5VT | Default: PA8  Alternate: CK\_OUT0, TIMER0\_CH0, I2C2\_SCL, USART0\_CK, USBFS\_SOF, SDIO\_D1, TLI\_R6, EVENTOUT, CTC\_SYNC |
| PA9 | 68 | I/O | 5VT | Default: PA9  Alternate: TIMER0\_CH1, I2C2\_SMBA, SPI1\_SCK, I2S1\_CK, USART0\_TX, SDIO\_D2, DCI\_D0, EVENTOUT Additional: USBFS\_VBUS |
| PA10 | 69 | I/O | 5VT | Default: PA10  Alternate: TIMER0\_CH2, SPI4\_MOSI, USART0\_RX,  USBFS\_ID, DCI\_D1, EVENTOUT, I2C2\_TXFRAME |
| PA11 | 70 | I/O | 5VT | Default: PA11  Alternate: TIMER0\_CH3, SPI3\_MISO, USART0\_CTS, USART5\_TX, CAN0\_RX, USBFS\_DM, TLI\_R4, EVENTOUT |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx LQFP100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
| PA12 | 71 | I/O | 5VT | Default: PA12  Alternate: TIMER0\_ETI, SPI4\_MISO, USART0\_RTS, USART5\_RX, CAN0\_TX, USBFS\_DP, TLI\_R5, EVENTOUT |
| PA13 | 72 | I/O | 5VT | Default: JTMS, SWDIO, PA13  Alternate: EVENTOUT |
| NC | 73 | - | - | - |
| VSS | 74 | P | - | Default: VSS |
| VDD | 75 | P | - | Default: VDD |
| PA14 | 76 | I/O | 5VT | Default: JTCK, SWCLK, PA14  Alternate: EVENTOUT |
| PA15 | 77 | I/O | 5VT | Default: JTDI, PA15  Alternate: TIMER1\_CH0, TIMER1\_ETI, SPI0\_NSS,  SPI2\_NSS, I2S2\_WS, USART0\_TX, EVENTOUT |
| PC10 | 78 | I/O | 5VT | Default: PC10  Alternate: SPI2\_SCK, I2S2\_CK, USART2\_TX, UART3\_TX,  SDIO\_D2, DCI\_D8, TLI\_R2, EVENTOUT |
| PC11 | 79 | I/O | 5VT | Default: PC11  Alternate: I2S2\_ADD\_SD, SPI2\_MISO, USART2\_RX,  UART3\_RX, SDIO\_D3, DCI\_D4, EVENTOUT |
| PC12 | 80 | I/O | 5VT | Default: PC12  Alternate: I2C1\_SDA, SPI2\_MOSI, I2S2\_SD, USART2\_CK,  UART4\_TX, SDIO\_CK, DCI\_D9, EVENTOUT |
| PD0 | 81 | I/O | 5VT | Default: PD0  Alternate: SPI3\_MISO, SPI2\_MOSI, I2S2\_SD, CAN0\_RX,  EXMC\_D2, EVENTOUT |
| PD1 | 82 | I/O | 5VT | Default: PD1  Alternate: SPI1\_NSS, I2S1\_WS, CAN0\_TX, EXMC\_D3,  EVENTOUT |
| PD2 | 83 | I/O | 5VT | Default: PD2  Alternate: TIMER2\_ETI, UART4\_RX, SDIO\_CMD,  DCI\_D11, EVENTOUT |
| PD3 | 84 | I/O | 5VT | Default: PD3  Alternate: SPI1\_SCK, I2S1\_CK, USART1\_CTS,  EXMC\_CLK, DCI\_D5, TLI\_G7, EVENTOUT |
| PD4 | 85 | I/O | 5VT | Default: PD4  Alternate: USART1\_RTS, EXMC\_NOE, EVENTOUT |
| PD5 | 86 | I/O | 5VT | Default: PD5  Alternate: USART1\_TX, EXMC\_NWE, EVENTOUT |
| PD6 | 87 | I/O | 5VT | Default: PD6  Alternate: SPI2\_MOSI, I2S2\_SD, USART1\_RX,  EXMC\_NWAIT, DCI\_D10, TLI\_B2, EVENTOUT |
| PD7 | 88 | I/O | 5VT | Default: PD7  Alternate: USART1\_CK, EXMC\_NE0, EXMC\_NCE1, |

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| --- | --- | --- | --- | --- | --- |
|  | **GD32F470Vx LQFP100** | | | | |
| **Pin Name** | **Pins** | **Pin**  **Type(1)** | **I/O**  **Level(2)** | **Functions description** |
|  |  |  |  | EVENTOUT |
| PB3 | 89 | I/O | 5VT | Default: JTDO, PB3  Alternate: TRACESWO, TIMER1\_CH1, SPI0\_SCK, SPI2\_SCK, I2S2\_CK, USART0\_RX, I2C1\_SDA, EVENTOUT |
| PB4 | 90 | I/O | 5VT | Default: JNTRST, PB4  Alternate: TIMER2\_CH0, SPI0\_MISO, SPI2\_MISO, I2S2\_ADD\_SD, I2C2\_SDA, SDIO\_D0, EVENTOUT, I2C0\_TXFRAME |
| PB5 | 91 | I/O | 5VT | Default: PB5  Alternate: TIMER2\_CH1, I2C0\_SMBA, SPI0\_MOSI, SPI2\_MOSI, I2S2\_SD, CAN1\_RX, USBHS\_ULPI\_D7, ENET\_PPS\_OUT, DCI\_D10, EVENTOUT |
| PB6 | 92 | I/O | 5VT | Default: PB6  Alternate: TIMER3\_CH0, I2C0\_SCL, USART0\_TX,  CAN1\_TX, DCI\_D5, EVENTOUT |
| PB7 | 93 | I/O | 5VT | Default: PB7  Alternate: TIMER3\_CH1, I2C0\_SDA, USART0\_RX,  EXMC\_NL/EXMC\_NADV, DCI\_VSYNC, EVENTOUT |
| BOOT0 | 94 | I/O | 5VT | Default: BOOT0 |
| PB8 | 95 | I/O | 5VT | Default: PB8  Alternate: TIMER1\_CH0, TIMER1\_ETI, TIMER3\_CH2, TIMER9\_CH0, I2C0\_SCL, SPI4\_MOSI, CAN0\_RX, ENET\_MII\_TXD3, SDIO\_D4, DCI\_D6, TLI\_B6, EVENTOUT |
| PB9 | 96 | I/O | 5VT | Default: PB9  Alternate: TIMER1\_CH1, TIMER3\_CH3, TIMER10\_CH0, I2C0\_SDA, SPI1\_NSS, I2S1\_WS, CAN0\_TX, SDIO\_D5, DCI\_D7, TLI\_B7, EVENTOUT |
| PE0 | 97 | I/O | 5VT | Default: PE0  Alternate: TIMER3\_ETI, UART7\_RX, EXMC\_NBL0,  DCI\_D2, EVENTOUT |
| PE1 | 98 | I/O | 5VT | Default: PE1  Alternate: TIMER0\_CH1\_ON, UART7\_TX, EXMC\_NBL1,  DCI\_D3, EVENTOUT |
| VSS | 99 | P | - | Default: VSS |
| VDD | 100 | P | - | Default: VDD |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

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**2.6.5.**

**GD32F470xx pin alternate functions**

**Table 2-7. Port A alternate functions summary**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PA0** |  | TIMER1\_C  H0/TIMER  1\_ETI | TIMER4\_C  H0 | TIMER7\_E  TI |  |  |  | USART1\_  CTS | UART3\_TX |  |  | ENET\_MII  \_CRS |  |  |  | EVENTOU  T |
| **PA1** |  | TIMER1\_C  H1 | TIMER4\_C  H1 |  |  | SPI3\_MOS  I |  | USART1\_  RTS | UART3\_R  X |  |  | ENET\_MII \_RX\_CLK/ ENET\_RMI I\_REF\_CL  K |  |  |  | EVENTOU  T |
| **PA2** |  | TIMER1\_C  H2 | TIMER4\_C  H2 | TIMER8\_C  H0 |  | I2S\_CKIN |  | USART1\_T  X |  |  |  | ENET\_MDI  O |  |  |  | EVENTOU  T |
| **PA3** |  | TIMER1\_C  H3 | TIMER4\_C  H3 | TIMER8\_C  H1 |  | I2S1\_MCK |  | USART1\_  RX |  |  | USBHS\_U  LPI\_D0 | ENET\_MII  \_COL |  |  | TLI\_B5 | EVENTOU  T |
| **PA4** |  |  |  |  |  | SPI0\_NSS | SPI2\_NSS/  I2S2\_WS | USART1\_  CK |  |  |  |  | USBHS\_S  OF | DCI\_HSYN  C | TLI\_VSYN  C | EVENTOU  T |
| **PA5** |  | TIMER1\_C  H0/TIMER  1\_ETI |  | TIMER7\_C  H0\_ON |  | SPI0\_SCK |  |  |  |  | USBHS\_U  LPI\_CK |  |  |  |  | EVENTOU  T |
| **PA6** |  | TIMER0\_B  RKIN | TIMER2\_C  H0 | TIMER7\_B  RKIN |  | SPI0\_MIS  O | I2S1\_MCK |  |  | TIMER12\_  CH0 |  |  | SDIO\_CM  D | DCI\_PIXC  LK | TLI\_G2 | EVENTOU  T |
| **PA7** |  | TIMER0\_C  H0\_ON | TIMER2\_C  H1 | TIMER7\_C  H0\_ON |  | SPI0\_MOS  I |  |  |  | TIMER13\_  CH0 |  | ENET\_MII \_RX\_DV/E NET\_RMII \_CRS\_DV | EXMC\_SD  NWE |  |  | EVENTOU  T |
| **PA8** | CK\_OUT0 | TIMER0\_C  H0 |  |  | I2C2\_SCL |  |  | USART0\_  CK |  | CTC\_SYN  C | USBFS\_S  OF |  | SDIO\_D1 |  | TLI\_R6 | EVENTOU  T |
| **PA9** |  | TIMER0\_C  H1 |  |  | I2C2\_SMB  A | SPI1\_SCK/  I2S1\_CK |  | USART0\_T  X |  |  |  |  | SDIO\_D2 | DCI\_D0 |  | EVENTOU  T |
| **PA10** |  | TIMER0\_C  H2 |  |  | I2C2\_TXF  RAME |  | SPI4\_MOS  I | USART0\_  RX |  |  | USBFS\_ID |  |  | DCI\_D1 |  | EVENTOU  T |
| **PA11** |  | TIMER0\_C  H3 |  |  |  |  | SPI3\_MIS  O | USART0\_  CTS | USART5\_T  X | CAN0\_RX | USBFS\_D  M |  |  |  | TLI\_R4 | EVENTOU  T |
| **PA12** |  | TIMER0\_E  TI |  |  |  |  | SPI4\_MIS  O | USART0\_  RTS | USART5\_  RX | CAN0\_TX | USBFS\_D  P |  |  |  | TLI\_R5 | EVENTOU  T |
| **PA13** | JTMS/SW  DIO |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EVENTOU  T |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PA14** | JTCK/SWC  LK |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EVENTOU  T |
| **PA15** | JTDI | TIMER1\_C  H0/TIMER  1\_ETI |  |  |  | SPI0\_NSS | SPI2\_NSS/  I2S2\_WS | USART0\_T  X |  |  |  |  |  |  |  | EVENTOU  T |

**Table 2-8. Port B alternate functions summary**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PB0** |  | TIMER0\_C  H1\_ON | TIMER2\_C  H2 | TIMER7\_C  H1\_ON |  |  | SPI4\_SCK | SPI2\_MOS  I/I2S2\_SD |  | TLI\_R3 | USBHS\_U  LPI\_D1 | ENET\_MII  \_RXD2 | SDIO\_D1 |  |  | EVENTOU  T |
| **PB1** |  | TIMER0\_C  H2\_ON | TIMER2\_C  H3 | TIMER7\_C  H2\_ON |  |  | SPI4\_NSS |  |  | TLI\_R6 | USBHS\_U  LPI\_D2 | ENET\_MII  \_RXD3 | SDIO\_D2 |  |  | EVENTOU  T |
| **PB2** |  | TIMER1\_C  H3 |  |  |  |  |  | SPI2\_MOS  I/I2S2\_SD |  |  | USBHS\_U  LPI\_D4 |  | SDIO\_CK |  |  | EVENTOU  T |
| **PB3** | JTDO/TRA  CESWO | TIMER1\_C  H1 |  |  |  | SPI0\_SCK | SPI2\_SCK/  I2S2\_CK | USART0\_  RX |  | I2C1\_SDA |  |  |  |  |  | EVENTOU  T |
| **PB4** | NJTRST |  | TIMER2\_C  H0 |  | I2C0\_TXF  RAME | SPI0\_MIS  O | SPI2\_MIS  O | I2S2\_ADD  \_SD |  | I2C2\_SDA |  |  | SDIO\_D0 |  |  | EVENTOU  T |
| **PB5** |  |  | TIMER2\_C  H1 |  | I2C0\_SMB  A | SPI0\_MOS  I | SPI2\_MOS  I/I2S2\_SD |  |  | CAN1\_RX | USBHS\_U  LPI\_D7 | ENET\_PP  S\_OUT | EXMC\_SD  CKE1 | DCI\_D10 |  | EVENTOU  T |
| **PB6** |  |  | TIMER3\_C  H0 |  | I2C0\_SCL |  |  | USART0\_T  X |  | CAN1\_TX |  |  | EXMC\_SD  NE1 | DCI\_D5 |  | EVENTOU  T |
| **PB7** |  |  | TIMER3\_C H1 |  | I2C0\_SDA |  |  | USART0\_  RX |  |  |  |  | EXMC\_NL/  EXMC\_NA  DV | DCI\_VSYN  C |  | EVENTOU  T |
| **PB8** |  | TIMER1\_C H0/TIMER  1\_ETI | TIMER3\_C H2 | TIMER9\_C H0 | I2C0\_SCL |  | SPI4\_MOS  I |  |  | CAN0\_RX |  | ENET\_MII  \_TXD3 | SDIO\_D4 | DCI\_D6 | TLI\_B6 | EVENTOU  T |
| **PB9** |  | TIMER1\_C  H1 | TIMER3\_C  H3 | TIMER10\_  CH0 | I2C0\_SDA | SPI1\_NSS/  I2S1\_WS |  |  |  | CAN0\_TX |  |  | SDIO\_D5 | DCI\_D7 | TLI\_B7 | EVENTOU  T |
| **PB10** |  | TIMER1\_C  H2 |  |  | I2C1\_SCL | SPI1\_SCK/  I2S1\_CK | I2S2\_MCK | USART2\_T  X |  |  | USBHS\_U  LPI\_D3 | ENET\_MII  \_RX\_ER | SDIO\_D7 |  | TLI\_G4 | EVENTOU  T |
| **PB11** |  | TIMER1\_C H3 |  |  | I2C1\_SDA | I2S\_CKIN |  | USART2\_  RX |  |  | USBHS\_U  LPI\_D4 | ENET\_MII \_TX\_EN/E NET\_RMII  \_TX\_EN |  |  | TLI\_G5 | EVENTOU  T |
| **PB12** |  | TIMER0\_B  RKIN |  |  | I2C1\_SMB  A | SPI1\_NSS/  I2S1\_WS | SPI3\_NSS | USART2\_  CK |  | CAN1\_RX | USBHS\_U  LPI\_D5 | ENET\_MII \_TXD0/EN ET\_RMII\_T  XD0 | USBHS\_ID |  |  | EVENTOU  T |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PB13** |  | TIMER0\_C H0\_ON |  |  | I2C1\_TXF  RAME | SPI1\_SCK/  I2S1\_CK | SPI3\_SCK | USART2\_  CTS |  | CAN1\_TX | USBHS\_U  LPI\_D6 | ENET\_MII \_TXD1/EN ET\_RMII\_T  XD1 |  |  |  | EVENTOU  T |
| **PB14** |  | TIMER0\_C  H1\_ON |  | TIMER7\_C  H1\_ON |  | SPI1\_MIS  O | I2S1\_ADD  \_SD | USART2\_  RTS |  | TIMER11\_  CH0 |  |  | USBHS\_D  M |  |  | EVENTOU  T |
| **PB15** | RTC\_REFI  N | TIMER0\_C H2\_ON |  | TIMER7\_C H2\_ON |  | SPI1\_MOS I/I2S1\_SD |  |  |  | TIMER11\_  CH1 |  |  | USBHS\_D  P |  |  | EVENTOU  T |

**Table 2-9. Port C alternate functions summary**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PC0** |  |  |  |  |  |  |  |  |  |  | USBHS\_U  LPI\_STP |  | EXMC\_SD  NWE |  |  | EVENTOU  T |
| **PC1** |  |  |  |  |  | SPI2\_MOS  I/I2S2\_SD |  | SPI1\_MOS  I/I2S1\_SD |  |  |  | ENET\_MD  C |  |  |  | EVENTOU  T |
| **PC2** |  |  |  |  |  | SPI1\_MIS  O | I2S1\_ADD  \_SD |  |  |  | USBHS\_U  LPI\_DIR | ENET\_MII  \_TXD2 | EXMC\_SD  NE0 |  |  | EVENTOU  T |
| **PC3** |  |  |  |  |  | SPI1\_MOS  I/I2S1\_SD |  |  |  |  | USBHS\_U  LPI\_NXT | ENET\_MII  \_TX\_CLK | EXMC\_SD  CKE0 |  |  | EVENTOU  T |
| **PC4** |  |  |  |  |  |  |  |  |  |  |  | ENET\_MII \_RXD0/EN ET\_RMII\_  RXD0 | EXMC\_SD  NE0 |  |  | EVENTOU  T |
| **PC5** |  |  |  |  |  |  |  | USART2\_  RX |  |  |  | ENET\_MII \_RXD1/EN ET\_RMII\_  RXD1 | EXMC\_SD  CKE0 |  |  | EVENTOU  T |
| **PC6** |  |  | TIMER2\_C  H0 | TIMER7\_C  H0 |  | I2S1\_MCK |  |  | USART5\_T  X |  |  |  | SDIO\_D6 | DCI\_D0 | TLI\_HSYN  C | EVENTOU  T |
| **PC7** |  |  | TIMER2\_C  H1 | TIMER7\_C  H1 |  | SPI1\_SCK/  I2S1\_CK | I2S2\_MCK |  | USART5\_  RX |  |  |  | SDIO\_D7 | DCI\_D1 | TLI\_G6 | EVENTOU  T |
| **PC8** |  |  | TIMER2\_C  H2 | TIMER7\_C  H2 |  |  |  |  | USART5\_  CK |  |  |  | SDIO\_D0 | DCI\_D2 |  | EVENTOU  T |
| **PC9** | CK\_OUT1 |  | TIMER2\_C  H3 | TIMER7\_C  H3 | I2C2\_SDA | I2S\_CKIN |  |  |  |  |  |  | SDIO\_D1 | DCI\_D3 |  | EVENTOU  T |
| **PC10** |  |  |  |  |  |  | SPI2\_SCK/  I2S2\_CK | USART2\_T  X | UART3\_TX |  |  |  | SDIO\_D2 | DCI\_D8 | TLI\_R2 | EVENTOU  T |
| **PC11** |  |  |  |  |  | I2S2\_ADD  \_SD | SPI2\_MIS  O | USART2\_  RX | UART3\_R  X |  |  |  | SDIO\_D3 | DCI\_D4 |  | EVENTOU  T |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PC12** |  |  |  |  | I2C1\_SDA |  | SPI2\_MOS  I/I2S2\_SD | USART2\_  CK | UART4\_TX |  |  |  | SDIO\_CK | DCI\_D9 |  | EVENTOU  T |
| **PC13** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EVENTOU  T |
| **PC14** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EVENTOU  T |
| **PC15** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EVENTOU  T |

**Table 2-10. Port D alternate functions summary**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PD0** |  |  |  |  |  | SPI3\_MIS  O | SPI2\_MOS I/I2S2\_SD |  |  | CAN0\_RX |  |  | EXMC\_D2 |  |  | EVENTOU  T |
| **PD1** |  |  |  |  |  |  |  | SPI1\_NSS/  I2S1\_WS |  | CAN0\_TX |  |  | EXMC\_D3 |  |  | EVENTOU  T |
| **PD2** |  |  | TIMER2\_E  TI |  |  |  |  |  | UART4\_R  X |  |  |  | SDIO\_CM  D | DCI\_D11 |  | EVENTOU  T |
| **PD3** |  |  |  |  |  | SPI1\_SCK/  I2S1\_CK |  | USART1\_  CTS |  |  |  |  | EXMC\_CL  K | DCI\_D5 | TLI\_G7 | EVENTOU  T |
| **PD4** |  |  |  |  |  |  |  | USART1\_  RTS |  |  |  |  | EXMC\_NO  E |  |  | EVENTOU  T |
| **PD5** |  |  |  |  |  |  |  | USART1\_T  X |  |  |  |  | EXMC\_NW  E |  |  | EVENTOU  T |
| **PD6** |  |  |  |  |  | SPI2\_MOS I/I2S2\_SD |  | USART1\_  RX |  |  |  |  | EXMC\_NW  AIT | DCI\_D10 | TLI\_B2 | EVENTOU  T |
| **PD7** |  |  |  |  |  |  |  | USART1\_  CK |  |  |  |  | EXMC\_NE  0/EXMC\_N  CE1 |  |  | EVENTOU  T |
| **PD8** |  |  |  |  |  |  |  | USART2\_T  X |  |  |  |  | EXMC\_D1  3 |  |  | EVENTOU  T |
| **PD9** |  |  |  |  |  |  |  | USART2\_  RX |  |  |  |  | EXMC\_D1  4 |  |  | EVENTOU  T |
| **PD10** |  |  |  |  |  |  |  | USART2\_  CK |  |  |  |  | EXMC\_D1  5 |  | TLI\_B3 | EVENTOU  T |
| **PD11** |  |  |  |  |  |  |  | USART2\_  CTS |  |  |  |  | EXMC\_A1  6/EXMC\_C  LE |  |  | EVENTOU  T |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PD12** |  |  | TIMER3\_C H0 |  |  |  |  | USART2\_  RTS |  |  |  |  | EXMC\_A1  7/EXMC\_A  LE |  |  | EVENTOU  T |
| **PD13** |  |  | TIMER3\_C H1 |  |  |  |  |  |  |  |  |  | EXMC\_A1  8 |  |  | EVENTOU  T |
| **PD14** |  |  | TIMER3\_C H2 |  |  |  |  |  |  |  |  |  | EXMC\_D0 |  |  | EVENTOU  T |
| **PD15** | CTC\_SYN  C |  | TIMER3\_C H3 |  |  |  |  |  |  |  |  |  | EXMC\_D1 |  |  | EVENTOU  T |

**Table 2-11. Port E alternate functions summary**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PE0** |  |  | TIMER3\_E  TI |  |  |  |  |  | UART7\_R  X |  |  |  | EXMC\_NB  L0 | DCI\_D2 |  | EVENTOU  T |
| **PE1** |  | TIMER0\_C H1\_ON |  |  |  |  |  |  | UART7\_TX |  |  |  | EXMC\_NB  L1 | DCI\_D3 |  | EVENTOU  T |
| **PE2** |  |  |  |  |  | SPI3\_SCK |  |  |  |  |  | ENET\_MII  \_TXD3 | EXMC\_A2  3 |  |  | EVENTOU  T |
| **PE3** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A1  9 |  |  | EVENTOU  T |
| **PE4** |  |  |  |  |  | SPI3\_NSS |  |  |  |  |  |  | EXMC\_A2  0 | DCI\_D4 | TLI\_B0 | EVENTOU  T |
| **PE5** |  |  |  | TIMER8\_C H0 |  | SPI3\_MIS  O |  |  |  |  |  |  | EXMC\_A2  1 | DCI\_D6 | TLI\_G0 | EVENTOU  T |
| **PE6** |  |  |  | TIMER8\_C H1 |  | SPI3\_MOS  I |  |  |  |  |  |  | EXMC\_A2  2 | DCI\_D7 | TLI\_G1 | EVENTOU  T |
| **PE7** |  | TIMER0\_E  TI |  |  |  |  |  |  | UART6\_R  X |  |  |  | EXMC\_D4 |  |  | EVENTOU  T |
| **PE8** |  | TIMER0\_C H0\_ON |  |  |  |  |  |  | UART6\_TX |  |  |  | EXMC\_D5 |  |  | EVENTOU  T |
| **PE9** |  | TIMER0\_C H0 |  |  |  |  |  |  |  |  |  |  | EXMC\_D6 |  |  | EVENTOU  T |
| **PE10** |  | TIMER0\_C H1\_ON |  |  |  |  |  |  |  |  |  |  | EXMC\_D7 |  |  | EVENTOU  T |
| **PE11** |  | TIMER0\_C H1 |  |  |  | SPI3\_NSS | SPI4\_NSS |  |  |  |  |  | EXMC\_D8 |  | TLI\_G3 | EVENTOU  T |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PE12** |  | TIMER0\_C H2\_ON |  |  |  | SPI3\_SCK | SPI4\_SCK |  |  |  |  |  | EXMC\_D9 |  | TLI\_B4 | EVENTOU  T |
| **PE13** |  | TIMER0\_C H2 |  |  |  | SPI3\_MIS  O | SPI4\_MIS  O |  |  |  |  |  | EXMC\_D1  0 |  | TLI\_DE | EVENTOU  T |
| **PE14** |  | TIMER0\_C H3 |  |  |  | SPI3\_MOS  I | SPI4\_MOS  I |  |  |  |  |  | EXMC\_D1  1 |  | TLI\_PIXCL  K | EVENTOU  T |
| **PE15** |  | TIMER0\_B  RKIN |  |  |  |  |  |  |  |  |  |  | EXMC\_D1  2 |  | TLI\_R7 | EVENTOU  T |

**Table 2-12. Port F alternate functions summary**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PF0** | CTC\_SYN  C |  |  |  | I2C1\_SDA |  |  |  |  |  |  |  | EXMC\_A0 |  |  | EVENTOU  T |
| **PF1** |  |  |  |  | I2C1\_SCL |  |  |  |  |  |  |  | EXMC\_A1 |  |  | EVENTOU  T |
| **PF2** |  |  |  |  | I2C1\_SMB  A |  |  |  |  |  |  |  | EXMC\_A2 |  |  | EVENTOU  T |
| **PF3** |  |  |  |  | I2C1\_TXF  RAME |  |  |  |  |  |  |  | EXMC\_A3 |  |  | EVENTOU  T |
| **PF4** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A4 |  |  | EVENTOU  T |
| **PF5** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A5 |  |  | EVENTOU  T |
| **PF6** |  |  |  | TIMER9\_C H0 |  | SPI4\_NSS |  |  | UART6\_R  X |  |  |  | EXMC\_NI  ORD |  |  | EVENTOU  T |
| **PF7** |  |  |  | TIMER10\_  CH0 |  | SPI4\_SCK |  |  | UART6\_TX |  |  |  | EXMC\_NR  EG |  |  | EVENTOU  T |
| **PF8** |  |  |  |  |  | SPI4\_MIS  O |  |  |  | TIMER12\_  CH0 |  |  | EXMC\_NI  OWR |  |  | EVENTOU  T |
| **PF9** |  |  |  |  |  | SPI4\_MOS  I |  |  |  | TIMER13\_  CH0 |  |  | EXMC\_CD |  |  | EVENTOU  T |
| **PF10** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_INT  R | DCI\_D11 | TLI\_DE | EVENTOU  T |
| **PF11** |  |  |  |  |  | SPI4\_MOS  I |  |  |  |  |  |  | EXMC\_SD  NRAS | DCI\_D12 |  | EVENTOU  T |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PF12** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A6 |  |  | EVENTOU  T |
| **PF13** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A7 |  |  | EVENTOU  T |
| **PF14** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A8 |  |  | EVENTOU  T |
| **PF15** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A9 |  |  | EVENTOU  T |

**Table 2-13. Port G alternate functions summary**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PG0** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A1  0 |  |  | EVENTOU  T |
| **PG1** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A1  1 |  |  | EVENTOU  T |
| **PG2** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A1  2 |  |  | EVENTOU  T |
| **PG3** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A1  3 |  |  | EVENTOU  T |
| **PG4** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A1  4 |  |  | EVENTOU  T |
| **PG5** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_A1  5 |  |  | EVENTOU  T |
| **PG6** |  |  |  |  |  |  |  |  |  |  |  |  | EXMC\_INT  1 | DCI\_D12 | TLI\_R7 | EVENTOU  T |
| **PG7** |  |  |  |  |  |  |  |  | USART5\_  CK |  |  |  | EXMC\_INT  2 | DCI\_D13 | TLI\_PIXCL  K | EVENTOU  T |
| **PG8** |  |  |  |  |  | SPI5\_NSS |  |  | USART5\_  RTS |  |  | ENET\_PP  S\_OUT | EXMC\_SD  CLK |  |  | EVENTOU  T |
| **PG9** |  |  |  |  |  |  |  |  | USART5\_  RX |  |  |  | EXMC\_NE  1/EXMC\_N  CE2 | DCI\_VSYN  C |  | EVENTOU  T |
| **PG10** |  |  |  |  |  | SPI5\_IO2 |  |  |  | TLI\_G3 |  |  | EXMC\_NC  E3\_0/EXM  C\_NE2 | DCI\_D2 | TLI\_B2 | EVENTOU  T |
| **PG11** |  |  |  |  |  | SPI5\_IO3 | SPI3\_SCK |  |  |  |  | ENET\_MII \_TX\_EN/E NET\_RMII  \_TX\_EN | EXMC\_NC  E3\_1 | DCI\_D3 | TLI\_B3 | EVENTOU  T |

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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PG12** |  |  |  |  |  | SPI5\_MIS  O | SPI3\_MIS  O |  | USART5\_  RTS | TLI\_B4 |  |  | EXMC\_NE  3 |  | TLI\_B1 | EVENTOU  T |
| **PG13** |  |  |  |  |  | SPI5\_SCK | SPI3\_MOS  I |  | USART5\_  CTS |  |  | ENET\_MII \_TXD0/EN ET\_RMII\_T  XD0 | EXMC\_A2  4 |  |  | EVENTOU  T |
| **PG14** |  |  |  |  |  | SPI5\_MOS  I | SPI3\_NSS |  | USART5\_T  X |  |  | ENET\_MII \_TXD1/EN ET\_RMII\_T  XD1 | EXMC\_A2  5 |  |  | EVENTOU  T |
| **PG15** |  |  |  |  |  |  |  |  | USART5\_  CTS |  |  |  | EXMC\_SD  NCAS | DCI\_D13 |  | EVENTOU  T |

**Table 2-14. Port H alternate functions summary**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PH0** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EVENTOU  T |
| **PH1** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EVENTOU  T |
| **PH2** |  |  |  |  |  |  |  |  |  |  |  | ENET\_MII  \_CRS | EXMC\_SD  CKE0 |  | TLI\_R0 | EVENTOU  T |
| **PH3** |  |  |  |  | I2C1\_TXF  RAME |  |  |  |  |  |  | ENET\_MII  \_COL | EXMC\_SD  NE0 |  | TLI\_R1 | EVENTOU  T |
| **PH4** |  |  |  |  | I2C1\_SCL |  |  |  |  |  | USBHS\_U  LPI\_NXT |  |  |  |  | EVENTOU  T |
| **PH5** |  |  |  |  | I2C1\_SDA | SPI4\_NSS |  |  |  |  |  |  | EXMC\_SD  NWE |  |  | EVENTOU  T |
| **PH6** |  |  |  |  | I2C1\_SMB  A | SPI4\_SCK |  |  |  | TIMER11\_  CH0 |  | ENET\_MII  \_RXD2 | EXMC\_SD  NE1 | DCI\_D8 |  | EVENTOU  T |
| **PH7** |  |  |  |  | I2C2\_SCL | SPI4\_MIS  O |  |  |  |  |  | ENET\_MII  \_RXD3 | EXMC\_SD  CKE1 | DCI\_D9 |  | EVENTOU  T |
| **PH8** |  |  |  |  | I2C2\_SDA |  |  |  |  |  |  |  | EXMC\_D1  6 | DCI\_HSYN  C | TLI\_R2 | EVENTOU  T |
| **PH9** |  |  |  |  | I2C2\_SMB  A |  |  |  |  | TIMER11\_  CH1 |  |  | EXMC\_D1  7 | DCI\_D0 | TLI\_R3 | EVENTOU  T |
| **PH10** |  |  | TIMER4\_C H0 |  | I2C2\_TXF  RAME |  |  |  |  |  |  |  | EXMC\_D1  8 | DCI\_D1 | TLI\_R4 | EVENTOU  T |

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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PH11** |  |  | TIMER4\_C H1 |  |  |  |  |  |  |  |  |  | EXMC\_D1  9 | DCI\_D2 | TLI\_R5 | EVENTOU  T |
| **PH12** |  |  | TIMER4\_C H2 |  |  |  |  |  |  |  |  |  | EXMC\_D2  0 | DCI\_D3 | TLI\_R6 | EVENTOU  T |
| **PH13** |  |  |  | TIMER7\_C H0\_ON |  |  |  |  |  | CAN0\_TX |  |  | EXMC\_D2  1 |  | TLI\_G2 | EVENTOU  T |
| **PH14** |  |  |  | TIMER7\_C H1\_ON |  |  |  |  |  |  |  |  | EXMC\_D2  2 | DCI\_D4 | TLI\_G3 | EVENTOU  T |
| **PH15** |  |  |  | TIMER7\_C H2\_ON |  |  |  |  |  |  |  |  | EXMC\_D2  3 | DCI\_D11 | TLI\_G4 | EVENTOU  T |

**Table 2-15. Port I alternate functions summary**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PI0** |  |  | TIMER4\_C H3 |  |  | SPI1\_NSS/  I2S1\_WS |  |  |  |  |  |  | EXMC\_D2  4 | DCI\_D13 | TLI\_G5 | EVENTOU  T |
| **PI1** |  |  |  |  |  | SPI1\_SCK/  I2S1\_CK |  |  |  |  |  |  | EXMC\_D2  5 | DCI\_D8 | TLI\_G6 | EVENTOU  T |
| **PI2** |  |  |  | TIMER7\_C H3 |  | SPI1\_MIS  O | I2S1\_ADD  \_SD |  |  |  |  |  | EXMC\_D2  6 | DCI\_D9 | TLI\_G7 | EVENTOU  T |
| **PI3** |  |  |  | TIMER7\_E  TI |  | SPI1\_MOS I/I2S1\_SD |  |  |  |  |  |  | EXMC\_D2  7 | DCI\_D10 |  | EVENTOU  T |
| **PI4** |  |  |  | TIMER7\_B  RKIN |  |  |  |  |  |  |  |  | EXMC\_NB  L2 | DCI\_D5 | TLI\_B4 | EVENTOU  T |
| **PI5** |  |  |  | TIMER7\_C H0 |  |  |  |  |  |  |  |  | EXMC\_NB  L3 | DCI\_VSYN  C | TLI\_B5 | EVENTOU  T |
| **PI6** |  |  |  | TIMER7\_C H1 |  |  |  |  |  |  |  |  | EXMC\_D2  8 | DCI\_D6 | TLI\_B6 | EVENTOU  T |
| **PI7** |  |  |  | TIMER7\_C H2 |  |  |  |  |  |  |  |  | EXMC\_D2  9 | DCI\_D7 | TLI\_B7 | EVENTOU  T |
| **PI8** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EVENTOU  T |
| **PI9** |  |  |  |  |  |  |  |  |  | CAN0\_RX |  |  | EXMC\_D3  0 |  | TLI\_VSYN  C | EVENTOU  T |
| **PI10** |  |  |  |  |  |  |  |  |  |  |  | ENET\_MII \_RX\_ER | EXMC\_D3  1 |  | TLI\_HSYN  C | EVENTOU  T |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **AF0** | **AF1** | **AF2** | **AF3** | **AF4** | **AF5** | **AF6** | **AF7** | **AF8** | **AF9** | **AF10** | **AF11** | **AF12** | **AF13** | **AF14** | **AF15** |
| **PI11** |  |  |  |  |  |  |  |  |  |  | USBHS\_U  LPI\_DIR |  |  |  |  | EVENTOU  T |

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**3.** **Functional description**

**3.1.**

**Arm® Cortex®-M4 core**

The Arm® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit Arm® Cortex®-M4 processor core

 Up to 240 MHz operation frequency

 Single-cycle multiplication and hardware divider

 Floating Point Unit (FPU)

 Integrated DSP instructions

 Integrated Nested Vectored Interrupt Controller (NVIC)

 24-bit SysTick timer

The Cortex®-M4 processor is based on the Armv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

 Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)

 Nested Vectored Interrupt Controller (NVIC)

 Flash Patch and Breakpoint (FPB)

 Data Watchpoint and Trace (DWT)

 Instrument Trace Macrocell (ITM)

 Memory Protection Unit (MPU)

 Serial Wire JTAG Debug Port (SWJ-DP)

 Trace Port Interface Unit (TPIU)

**3.2.**

**On-chip memory**

 Up to 3072 Kbytes of Flash memory, including code Flash and data Flash.

 The region of the MCU executing instructions without waiting time is up to 1024K bytes (in case that Flash size equal to 512K, all memory is no waiting time). A long delay when CPU fetches the instructions out of the range.

 256 KB to 768 KB of SRAM.

The Arm® Cortex®-M4 processor is structured in Harvard architecture which can use separate

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GD32F470xx Datasheet buses to fetch instructions and load/store data. 3072 Kbytes of inner Flash at most, which includes code Flash and data Flash is available for storing programs and data, and there is no waiting time within code Flash area when CPU executes instructions. Up to 768 Kbytes of inner SRAM is composed of SRAM0 (112KB), SRAM1 (16KB), and SRAM2 (64KB) and ADDSRAM (512KB) that can be accessed at same time, and including 64 KB of TCM (tightly- coupled memory) data RAM that can be accessed only by the data bus of the Cortex®-M4 core. The additional 4KB of backup SRAM (BKP SRAM) is implemented in the backup domain, which can keep its content even when the VDD power supply is down. [***Table***](#PageMark15)[***2-2.***](#PageMark15)[***GD32F470xx***](#PageMark15)[***memory***](#PageMark15)[***map***](#PageMark15)shows the memory map of the GD32F470xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

**3.3.**

**Clock, reset and supply management**

 Internal 16 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator

 Internal 48 MHz RC oscillator

 Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator

 Integrated system clock PLL

 2.6 to 3.6 V application supply and I/Os

 Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 240 MHz. The maximum frequency of the two APB domains including APB1 is 60 MHz and APB2 is 120 MHz. See [***Figure***](#PageMark18)[***2-6.***](#PageMark18)[***GD32F470xx***](#PageMark18)[***clock***](#PageMark18)[***tree***](#PageMark18)for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.4 V and down to 1.8V. The device remains in reset mode when VDD is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

 VDD range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator.

Provided externally through VDD pins.

 VSSA, VDDA range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. VDDA and VSSA must be connected to VDD and VSS, respectively.

 VBAT range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when VDD is not present.

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**3.4.**

**Boot modes**

At startup, boot pins are used to select one of three boot options:

 Boot from main Flash memory (default)

 Boot from system memory

 Boot from on-chip SRAM

The boot loader is located in the internal 30KB of information blocks for the boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART2 (PB10 and PB11, or PC10 and PC11), and USBFS (PA9, PA10, PA11 and PA12) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 0 of Flash memory is selected. It also supports to boot from bank 1 of Flash memory by setting a bit in option bytes.

**3.5.**

**Power saving modes**

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

 **Sleep** mode

In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

 **Deep-sleep** mode

In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC16M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC Tamper and TimeStamp event, the LVD output, ENET wakeup, RTC wakeup and USB wakeup. When exiting the deep-sleep mode, the IRC16M is selected as the system clock.

 **Standby** mode

In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC16M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, and the rising edge on WKUP pin.

**3.6.**

**Analog to digital converter (ADC)**

 12-bit SAR ADC's conversion rate is up to 2.6 MSPS

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 12-bit, 10-bit, 8-bit or 6-bit configurable resolution

 Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit

 Input voltage range: VSSA to VDDA (2.6 V ≤ VDDA ≤ 3.6 V)

 Temperature sensor

Up to three 12-bit 2.6 MSPS multi-channel ADCs are integrated in the device. It has a total of

19 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor (VSENSE), 1 channel for internal reference voltage (VREFINT) and 1 channel for external battery power supply (VBAT). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timers (TIMER0 and TIMER7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC\_IN16 input channel which is used to convert the sensor output voltage in a digital value.

**3.7.**

**Digital to analog converter (DAC)**

 Two 12-bit DAC converter of independent output channel

 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is VREFP.

**3.8.**

**DMA**

 16 channels DMA controller and each channel are configurable (8 for DMA0 and 8 for

DMA1)

 Support independent 8, 16, 32-bit memory and peripheral transfer

 Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, UARTs, DAC, I2S, SDIO and DCI

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel

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GD32F470xx Datasheet requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

**3.9.**

**General-purpose inputs/outputs (GPIOs)**

 Up to 140 fast GPIOs, all mappable on 16 external interrupt lines

 Analog input/output configurable

 Alternate function input/output configurable

There are up to 140 general purpose I/O pins (GPIO) in GD32F470xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH15 and PI0 ~ PI11 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

**3.10.**

**Timers and PWM generation**

 Two 16-bit advanced timer (TIMER0 & TIMER7), eight 16-bit general timers (TIMER2, TIMER3, TIMER8 ~ TIMER13), two 32-bit general timers (TIMER1 & TIMER4) and two 16-bit basic timer (TIMER5 & TIMER6)

 Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input

 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match

 Encoder interface controller with two inputs using quadrature decoder

 24-bit SysTick timer down counter

 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as a single pulse generation

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or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 &

TIMER4 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 &

TIMER3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER8 ~ TIMER13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F470xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

 A 24-bit down counter

 Auto reload capability

 Maskable system interrupt generation when the counter reaches 0

 Programmable clock source

**3.11.**

**Real time clock (RTC) and backup registers**

 Independent binary-coded decimal (BCD) format timer/counter with twenty 32-bit backup registers.

 Calendar with sub-second, seconds, minutes, hours, week day, date, year and month automatically correction

 Alarm function with wake up from deep-sleep and standby mode capability

 On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

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**3.12.**

**Inter-integrated circuit (I2C)**

 Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 400 KHz (Fast mode)

 Provide arbitration function, optional PEC (packet error checking) generation and checking

 Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to

400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

**3.13.**

**Serial peripheral interface (SPI)**

 Master or slave operation with full-duplex or simplex mode

 Support both master and slave mode

 Hardware CRC calculation and transmit automatic CRC error checking

 Quad wire configuration available in master mode (only in SPI5)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by

the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI5 (SPI5 is not available in GD32F470Vx series).

**3.14.**

**Universal synchronous/asynchronous receiver transmitter (USART/UART)**

 Maximum speed up to 15MBit/s for USART0 and USART5

 Maximum speed up to 7.5MBit/s for USART1, USART2, UART3, UART4, UART6 and UART7

 Supports both asynchronous and clocked synchronous serial communication modes

 IrDA SIR encoder and decoder support

 LIN break generation and detection

 ISO 7816-3 compliant smart card interface

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GD32F470xx Datasheet The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4, UART6, UART7) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

**3.15.**

**Inter-IC sound (I2S)**

 Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI1 and SPI2

 Support either master or slave mode Audio

 Sampling frequencies from 8 KHz up to 192 KHz are supported

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32F470xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequencies from 8 KHz to 192 KHz is supported.

**3.16.**

**Universal serial bus full-speed interface (USBFS)**

 One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s

 Internal 48 MHz oscillator support crystal-less operation

 Internal main PLL for USB CLK compliantly

 Internal USBFS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

**3.17.**

**Universal serial bus high-speed interface (USBHS)**

 One USB device/host/OTG high-speed Interface with frequency up to 480 Mbit/s

 An external PHY device connected to the ULPI is required when using in HS mode

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GD32F470xx Datasheet USBHS supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller provides ULPI interface for external USB PHY integration and it also contains a full-speed USB PHY internal. For full- speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. HUB connection is supported when USBHS operates at high-speed in host mode. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system.

**3.18.**

**Controller area network (CAN)**

 Two CAN2.0B interface with communication frequency up to 1 Mbit/s

 Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

**3.19.**

**Ethernet (ENET)**

 IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN

 10/100 Mbit/s rates with dedicated DMA controller and SRAM

 Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 16 with 25 MHz output and RMII up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

**3.20.**

**External memory controller (EXMC)**

 Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and CF card, SDRAM with up to 32-bit data bus

 Provide ECC calculating hardware module for NAND Flash memory block

 Two SDRAM banks with independent configuration, up to 13-bits Row Address, 11-bits

Column Address, 2-bits internal banks address

 SDRAM Memory size: 4x16Mx32bit (256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)

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GD32F470xx Datasheet External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC supports code execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

The EXMC of GD32F470xx in LQFP144 & BGA176 package also supports synchronous dynamic random access memory (SDRAM). It translates AHB transactions into the appropriate SDRAM protocol, and meanwhile, makes sure the access time requirements of the external SDRAM devices are satisfied.

**3.21.**

**Secure digital input and output card interface (SDIO)**

 Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

**3.22.**

**TFT LCD interface (TLI)**

 24-bit RGB Parallel Pixel Output; 8 bits-per-pixel (RGB888)

 Supports up to XVGA (1024x768) resolution

 2 display layers with dedicated FIFO (64x32-bit)

The TFT LCD interface provides a parallel digital RGB (Red, Green and Blue) and signals for horizontal, vertical synchronization, Pixel Clock and Data Enable as output to interface directly to a variety of LCD (Liquid Crystal Display) and TFT (Thin Film Transistor) panels. A built-in DMA engine continuously move data from system memory to TLI and then, output to an external LCD display. Two separate layers are supported in TLI, as well as layer window and blending function.

**3.23.**

**Image processing accelerator (IPA)**

 Copy one source image to the destination image

 Convert one source image to the destination image with specific pixel format

 Convert and blend two source images to the destination image with specific pixel format

 Fill up the destination image with a specific color

The Image processing accelerator (IPA) provides a configurable and flexible image format conversion from one or two source image to the destination image. Eleven pixel formats from 4-bit up to 32-bit per pixel independently for the two source images and five pixel formats from

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GD32F470xx Datasheet 16-bit up to 32-bit per pixel for the destination image are supported. Two 256\*32 bits Look- Up Tables (LUT) separately for the two source images are implemented for the indirect pixel formats.

**3.24.**

**Digital camera interface (DCI)**

 Digital video/picture capture

 8/10/12/14 data width supported

 High transfer efficiency with DMA interface

 Video/picture crop supported

 Various pixel formats supported including JPEG/YCrCb/RGB

 Hard/embedded synchronous signals supported

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

**3.25.**

**Debug mode**

 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

**3.26.**

**Package and operation temperature**

 BGA176 (GD32F470Ix), LQFP144 (GD32F470Zx), BGA100 (GD32F470Vx) and LQFP100 (GD32F470Vx)

 Operation temperature range: -40°C to +85°C (industrial level) for grade 6 devices, and -40°C to +105°C (industrial level) for grade 7 devices

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**4.** **Electrical characteristics**

**4.1.**

**Absolute maximum ratings**

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4-1. Absolute maximum ratings(1)(4)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| VDD | External voltage range(2) | VSS - 0.3 | VSS + 3.6 | V |
| VDDA | External analog supply voltage | VSSA - 0.3 | VSSA + 3.6 | V |
| VBAT | External battery supply voltage | VSS - 0.3 | VSS + 3.6 | V |
| VIN | Input voltage on 5V tolerant pin(3) | VSS - 0.3 | VDD + 3.6 | V |
| Input voltage on other I/O | VSS - 0.3 | 3.6 | V |
| |ΔVDDX| | Variations between different VDD power pins | — | 50 | mV |
| |VSSX −VSS| | Variations between different ground pins | — | 50 | mV |
| IIO | Maximum current for GPIO pins | — | ±25 | mA |
| TA | Operating temperature range for grade 6 device | -40 | +85 | °C |
| Operating temperature range for grade 7 device | -40 | +105 |
| PD | Power dissipation at TA = 85°C of BGA176(5) | — | 888 | mW |
| Power dissipation at TA = 85°C of LQFP144(5) | — | 820 |
| Power dissipation at TA = 85°C of BGA100(5) | — | 511 |
| Power dissipation at TA = 85°C of LQFP100(5) | — | 697 |
| Power dissipation at TA = 105°C of LQFP144(5) | — | 410 |
| Power dissipation at TA = 105°C of LQFP100(5) | — | 348 |
| TSTG | Storage temperature range | -65 | +150 | °C |
| TJ | Maximum junction temperature | — | 125 | °C |

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) VIN maximum value cannot exceed 5.5 V.

(4) It is recommended that VDD and VDDA are powered by the same source. The maximum difference between

VDD and VDDA does not exceed 300 mV during power-up and operation.

(5) For grade 6 devices, the parameter of TA=85°C, For grade 7 devices, the parameter of TA=105°C;

**4.2.**

**Recommended DC characteristics**

**Table 4-2. DC operating conditions**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min(1)** | **Typ** | **Max(1)** | **Unit** |
| VDD | Supply voltage | — | 2.6 | 3.3 | 3.6 | V |
| VDDA | Analog supply voltage | Same as VDD | 2.6 | 3.3 | 3.6 | V |

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|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min(1)** | **Typ** | **Max(1)** | **Unit** |  |
| VBAT | Battery supply voltage | — | 1.8**(2)** | — | 3.6 | V |

(1) Based on characterization, not tested in production.

(2) In the application which VBAT supply the backup domains, if the VBAT voltage drops below the minimum value,

when VDD is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

**Figure 4-1. Recommended power supply decoupling capacitors(1)(2)**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  | | |
|  |  | |
| **VBAT VSS**  **N \* VDD VSS**  **VDDA VSSA**  **VREFP VREFN** |  |
| 100 nF |
|  |
| 4.7 μF + N \* 100 nF |
|  |
|  |
| 1 μF 10 nF |
|  |
| 1 μF 10 nF |
|  |

(1) The VREFP and VREFN pins are only available on no less than 100-pin packages, or else the VREFP and

VREFN pins are not available and internally connected to VDDA and VSSA pins. More details refer to ***AN056 GD32F4xx Hardware Development Guide***.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

**Table 4-3. Clock frequency(1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| fHCLK | AHB clock frequency | — | — | 240 | MHz |
| fAPB1 | APB1 clock frequency | — | — | 60 | MHz |
| fAPB2 | APB2 clock frequency | — | — | 120 | MHz |

(1) Guaranteed by design, not tested in production.

**Table 4-4. Operating conditions at Power up / Power down(1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| tVDD | VDD rise time rate | — | 0 | ∞ | μs/V |
| VDD fall time rate | 20 | ∞ |

(1) Guaranteed by design, not tested in production.

**Table 4-5. Start-up timings of Operating conditions(1)(2)(3)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Typ** | **Unit** |
| tstart-up | Start-up time | Code area in FLASH = 512 KB | 138 | ms |
| Code area in FLASH = 768 KB | 203 |

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Typ** | **Unit** |  |
|  |  | Code area in FLASH = 1024 KB | 270 |  |

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

(3) PLL is off.

**Table 4-6. Power saving mode wakeup timings characteristics(1)(2)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Typ** | **Unit** |
| tSleep | Wakeup from Sleep mode | 0.623 | μs |
| tDeep-sleep | Wakeup from Deep-sleep mode（LDO On） | 1.57 |
| Wakeup from Deep-sleep mode  （LDO in low power mode） | 1.57 |
| tStandby | Wakeup from Standby mode | 140 | ms |

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first

instruction under the below conditions: VDD = VDDA = 3.3 V, IRC16M = System clock = 16 MHz.

**4.3.**

**Power consumption**

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

**Table 4-7. Power consumption characteristics(2)(3)(4)(5)(6)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ(1)** | **Max** | **Unit** |
| IDD+IDDA | Supply current  (Run mode) | VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 240 MHz, All peripherals  enabled | — | 73.5 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 240 MHz, All peripherals  disabled | — | 44.1 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 200 MHz, All peripherals  enabled | — | 61.5 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 200 MHz, All peripherals  disabled | — | 37.1 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 180 MHz, All peripherals  enabled | — | 55.9 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 180 MHz, All peripherals  disabled | — | 33.9 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 168 MHz, All peripherals  enabled | — | 52.6 | — | mA |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ(1)** | **Max** | **Unit** |
|  |  | VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 168 MHz, All peripherals  disabled | — | 32.0 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 120 MHz, All peripherals  enabled | — | 38.6 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 120 MHz, All peripherals  disabled | — | 23.9 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 108 MHz, All peripherals  enabled | — | 35.2 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 108 MHz, All peripherals  disabled | — | 22.0 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals  enabled | — | 29.9 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals  disabled | — | 19.0 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 60 MHz, All peripherals  enabled | — | 21.2 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals  disabled | — | 13.9 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals  enabled | — | 13.3 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals  disabled | — | 9.5 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 25 MHz, All peripherals  enabled | — | 11.7 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, All peripherals  disabled | — | 8.5 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals  enabled | — | 8.9 | — | mA |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ(1)** | **Max** | **Unit** |
|  |  | VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals  disabled | — | 6.9 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals  enabled | — | 6.4 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals  disabled | — | 5.3 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, All peripherals  enabled | — | 5.0 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 4 MHz, All peripherals  disabled | — | 4.5 | — | mA |
| Supply current (Sleep mode) | VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 240 MHz,CPU clock off, All  peripherals enabled | — | 50.0 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 240 MHz, CPU clock off,  All peripherals disabled | — | 21.7 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 200 MHz,CPU clock off, All  peripherals enabled | — | 42.2 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 200 MHz, CPU clock off,  All peripherals disabled | — | 18.7 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 180 MHz, CPU clock off,  All peripherals enabled | — | 38.5 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 180 MHz, CPU clock off,  All peripherals disabled | — | 17.2 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 168 MHz, CPU clock off,  All peripherals enabled | — | 36.2 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 168 MHz, CPU clock off,  All peripherals disabled | — | 16.4 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 120 MHz, CPU clock off,  All peripherals enabled | — | 27.0 | — | mA |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ(1)** | **Max** | **Unit** |
|  |  | VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 120 MHz, CPU clock off,  All peripherals disabled | — | 12.8 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 108 MHz, CPU clock off,  All peripherals enabled | — | 24.7 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 108 MHz, CPU clock off,  All peripherals disabled | — | 11.9 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All  peripherals enabled | — | 21.2 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All  peripherals disabled | — | 10.5 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All  peripherals enabled | — | 15.5 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All  peripherals disabled | — | 8.4 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 30 MHz, CPU clock off, All  peripherals enabled | — | 10.5 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All  peripherals disabled | — | 6.7 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, CPU clock off, All  peripherals enabled | — | 9.4 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, CPU clock off, All  peripherals disabled | — | 6.2 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 16 MHz, CPU clock off, All  peripherals enabled | — | 7.4 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, CPU clock off, All  peripherals disabled | — | 5.4 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 8 MHz, CPU clock off, All  peripherals enabled | — | 5.7 | — | mA |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ(1)** | **Max** | **Unit** |
|  |  | VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 8 MHz, CPU clock off, All  peripherals disabled | — | 4.7 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 4 MHz, CPU clock off, All  peripherals enabled | — | 4.8 | — | mA |
| VDD = VDDA = 3.3 V, HXTAL = 25 MHz,  System clock = 4 MHz, CPU clock off, All  peripherals disabled | — | 4.3 | — | mA |
| Supply current  (Deep-Sleep  mode) | VDD = VDDA = 3.3 V, LDO in run mode and  normal driver mode, IRC32K off, RTC off | — | 1.39 | — | mA |
| VDD = VDDA = 3.3 V, LDO in low power  mode and normal driver mode, IRC32K off | — | 1.36 | 11 | mA |
| VDD = VDDA = 3.3 V, LDO in run mode and  low driver mode, IRC32K off, RTC off | — | 1.33 | — | mA |
| VDD = VDDA = 3.3 V, LDO in low power  mode and low driver mode, IRC32K off | — | 1.30 | — | mA |
| Supply current (Standby mode) | VDD = VDDA = 3.3 V, LXTAL off, IRC32K on,  RTC on, backup SRAM LDO ON | — | 9.90 | 17.5 | μA |
| VDD = VDDA = 3.3 V, LXTAL off, IRC32K on,  RTC off, backup SRAM LDO ON | — | 9.67 | 17.3 | μA |
| VDD = VDDA = 3.3 V, LXTAL off, IRC32K off,  RTC off, backup SRAM LDO ON | — | 9.19 | 16.8 | μA |
| VDD = VDDA = 3.3 V, LXTAL off, IRC32K off,  RTC off, backup SRAM LDO OFF | — | 3.379 | 11 | μA |
| IBAT | Battery supply  current (Backup  mode) | VDD off, VDDA off, VBAT=3.6V, LXTAL on with external crystal, RTC on, LXTAL High  driving, backup SRAM LDO ON | — | 9.09 | — | μA |
| VDD off, VDDA off, VBAT =3.3V, LXTAL on with external crystal, RTC on, LXTAL High  driving, backup SRAM LDO ON | — | 8.93 | — | μA |
| VDD off, VDDA off, VBAT =2.6V, LXTAL on  with external crystal, RTC on, LXTAL High  driving, backup SRAM LDO ON | — | 8.74 | — | μA |
| VDD off, VDDA off, VBAT =1.8V, LXTAL on with external crystal, RTC on, LXTAL High  driving, backup SRAM LDO ON | — | 7.47 | — | μA |
| VDD off, VDDA off, VBAT =3.6V, LXTAL on with external crystal, RTC on, LXTAL High  driving, backup SRAM LDO OFF | — | 2.23 | — | μA |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ(1)** | **Max** | **Unit** |
|  |  | VDD off, VDDA off, VBAT =3.3V, LXTAL on with external crystal, RTC on, LXTAL High  driving, backup SRAM LDO OFF | — | 2.13 | — | μA |
| VDD off, VDDA off, VBAT =2.6V, LXTAL on with external crystal, RTC on, LXTAL High  driving, backup SRAM LDO OFF | — | 2 | — | μA |
| VDD off, VDDA off, VBAT =1.8V, LXTAL on with external crystal, RTC on, LXTAL High  driving, backup SRAM LDO OFF | — | 1.89 | — | μA |
| VDD off, VDDA off, VBAT =3.6V, LXTAL on  with external crystal, RTC on, LXTAL Low  driving, backup SRAM LDO ON | — | 8.16 | — | μA |
| VDD off, VDDA off, VBAT =3.3V, LXTAL on  with external crystal, RTC on, LXTAL Low  driving, backup SRAM LDO ON | — | 8 | — | μA |
| VDD off, VDDA off, VBAT =2.6V, LXTAL on  with external crystal, RTC on, LXTAL Low  driving, backup SRAM LDO ON | — | 7.8 | — | μA |
| VDD off, VDDA off, VBAT =1.8V, LXTAL on  with external crystal, RTC on, LXTAL Low  driving, backup SRAM LDO ON | — | 6.7 | — | μA |
| VDD off, VDDA off, VBAT =3.6V, LXTAL on  with external crystal, RTC on, LXTAL Low  driving, backup SRAM LDO OFF | — | 1.27 | — | μA |
| VDD off, VDDA off, VBAT =3.3V, LXTAL on  with external crystal, RTC on, LXTAL Low  driving, backup SRAM LDO OFF | — | 1.18 | — | μA |
| VDD off, VDDA off, VBAT =2.6V, LXTAL on  with external crystal, RTC on, LXTAL Low  driving, backup SRAM LDO OFF | — | 1.06 | — | μA |
| VDD off, VDDA off, VBAT =1.8V, LXTAL on  with external crystal, RTC on, LXTAL Low  driving, backup SRAM LDO OFF | — | 0.96 | — | μA |

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for TA = 25 ℃ and test result is mean value.

(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is

needed, no PLL.

(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is

closed, using PLL.

(5) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC16M, or IRC32K are ON, an

additional power consumption should be considered.

(6) All GPIOs are configured as analog mode except standby mode.

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**Figure 4-2. Typical supply current consumption in Run mode**

**Figure 4-3. Typical supply current consumption in Sleep mode**

**4.4.**

**EMC characteristics**

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in [***Table***](#PageMark83)[***4-8.***](#PageMark83)[***EMS***](#PageMark83)[***characteristics(1)***](#PageMark83), based on the EMS levels and classes compliant with IEC 61000 series standard.

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**Table 4-8. EMS characteristics(1)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Level/Class** |
| VESD | Voltage applied to all device pins to  induce a functional disturbance | VDD = 3.3 V, TA = 25 °C BGA176, fHCLK = 240 MHz conforms to IEC 61000-4-2 | 3A |
| VFTB | Fast transient voltage burst applied to  induce a functional disturbance through  100 pF on VDD and VSS pins | VDD = 3.3 V, TA = 25 °C BGA176, fHCLK = 240 MHz conforms to IEC 61000-4-4 | 3A |

(1) Based on characterization, not tested in production.

EMI (Electromagnetic Interference) emission test result is given in the [***Table***](#PageMark83)[***4-9.***](#PageMark83)[***EMI***](#PageMark83)[***characteristics*(1)**](#PageMark83), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

**Table 4-9. EMI characteristics(1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Tested**  **frequency band** | **Max vs.**  **[fHXTAL/fHCLK]** | **Unit** |
| **25/240 MHz** |
| SEMI | Peak level | VDD = 3.6 V, TA = +25 °C, LQFP144, f**HCLK** = 240 MHz, conforms to SAE  J1752-3:2017 | 0.15 MHz to 30 MHz | 3.15 | dBμV |
| 30 MHz to 130 MHz | 11.54 |
| 130 MHz to 1 GHz | 9.55 |

(1) Based on characterization, not tested in production.

**4.5.**

**Power supply supervisor characteristics**

**Table 4-10. Power supply supervisor characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| VLVD(1) | Low voltage  Detector level selection | LVDT<2:0> = 000(rising edge) | — | 2.1 | — | V |
| LVDT<2:0> = 000(falling edge) | — | 1.98 | — |
| LVDT<2:0> = 001(rising edge) | — | 2.23 | — |
| LVDT<2:0> = 001(falling edge) | — | 2.12 | — |
| LVDT<2:0> = 010(rising edge) | — | 2.36 | — |
| LVDT<2:0> = 010(falling edge) | — | 2.25 | — |
| LVDT<2:0> = 011(rising edge) | — | 2.50 | — |
| LVDT<2:0> = 011(falling edge) | — | 2.38 | — |
| LVDT<2:0> = 100(rising edge) | — | 2.62 | — |
| LVDT<2:0> = 100(falling edge) | — | 2.52 | — |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
|  |  | LVDT<2:0> = 101(rising edge) | — | 2.74 | — |  |
| LVDT<2:0> = 101(falling edge) | — | 2.66 | — |
| LVDT<2:0> = 110(rising edge) | — | 2.90 | — |
| LVDT<2:0> = 110(falling edge) | — | 2.80 | — |
| LVDT<2:0> = 111(rising edge) | — | 3.03 | — |
| LVDT<2:0> = 111(falling edge) | — | 2.93 | — |
| VLVDhyst(2) | LVD hystersis | — | — | 100 | — | mV |
| VPOR(1) | Power on reset threshold | — | — | 2.45 | — | V |
| VPDR(1) | Power down reset  threshold | — | — | 1.82 | — | V |
| VPDRhyst(2) | PDR hysteresis | — | — | 600 | — | mV |
| VBOR3(1) | Brownout level 3 threshold | Falling edge | — | 2.80 | — | V |
| Rising edge | — | 2.89 | — | V |
| VBOR2(1) | Brownout level 2 threshold | Falling edge | — | 2.51 | — | V |
| Rising edge | — | 2.59 | — | V |
| VBOR1(1) | Brownout level 1 threshold | Falling edge | — | 2.20 | — | V |
| Rising edge | — | 2.30 | — | V |
| VBORhyst(2) | BOR hysteresis | — | — | 100 | — | mV |
| tRSTTEMPO(2) | Reset temporization | — | — | 2 | — | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Figure 4-4. Recommended PDR\_ON pin circuit**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **VDD** | |  |  | |
| **PDR\_ON** |  |
| R  External |  |
| 10 kΩ |
|  |
| circuit |
|  | |
|  | | | | |

(1) The PDR supervisor can be enabled/disabled through PDR\_ON pin.

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(2) When PDR\_ON pin is connected to VSS (Internal Reset OFF), the VBAT functionality is no more available and

VBAT pin should be connected to VDD.

(3) The PDR\_ON pin must be kept at high level. The user can flexibly adjust the value of the pull-up resistor R

according to the specific scenario for a better performance.

**4.6.**

**Electrical sensitivity**

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

**Table 4-11. ESD characteristics(1)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| VESD(HBM) | Electrostatic discharge  voltage (human body model) | TA = 25 °C;  JS-001-2017 | — | — | 5000 | V |
| VESD(CDM) | Electrostatic discharge  voltage (charge device model) | TA = 25 °C;  JS-002-2018 | — | — | 1000 | V |

(1) Based on characterization, not tested in production.

**Table 4-12. Static latch-up characteristics(1)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| LU | I-test | TA = 105 °C; JESD78 | — | — | ±200 | mA |
| Vsupply over voltage | — | — | 5.4 | V |

(1) Based on characterization, not tested in production.

**4.7.**

**External clock characteristics**

**Table 4-13. High speed external clock (HXTAL) generated from a crystal/ceramic**

**characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fHXTAL(1) | Crystal or ceramic frequency | 2.6 V ≤VDD ≤ 3.6 V | 4 | 25 | 32 | MHz |
| RF(2) | Feedback resistor | VDD = 3.3 V | — | 400 | — | kΩ |
| CHXTAL(2) (3) | Recommended matching  capacitance on OSCIN and  OSCOUT | — | — | 20 | 30 | pF |
| Ducy(HXTAL)(2) | Crystal or ceramic duty cycle | — | 30 | 50 | 70 | % |
| gm(2) | Oscillator transconductance | Startup | — | 25 | — | mA/V |
| IDDHXTAL(1) | Crystal or ceramic operating  current | VDD = 3.3 V | — | 1.2 | — | mA |
| tSUHXTAL(1) | Crystal or ceramic startup time | VDD = 3.3 V | — | 0.42 | — | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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(3) CHXTAL1 = CHXTAL2 = 2\*(CLOAD - CS), For CHXTAL1 and CHXTAL2, it is recommended matching capacitance on OSCIN

and OSCOUT. For CLOAD, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For CS, it is PCB and MCU pin stray capacitance.

**Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fHXTAL\_ext(1) | External clock source or oscillator  frequency | 2.6 V ≤VDD ≤ 3.6  V | 1 | — | 50 | MHz |
| VHXTALH(2) | OSCIN input pin high level  voltage | VDD = 3.3 V | 0.7 VDD | — | VDD | V |
| VHXTALL(2) | OSCIN input pin low level voltage | VSS | — | 0.3 VDD | V |
| tH/L(HXTAL) (2) | OSCIN high or low time | — | 5 | — | — | ns |
| tR/F(HXTAL) (2) | OSCIN rise or fall time | — | — | — | 10 | ns |
| CIN(2) | OSCIN input capacitance | — | — | 5 | — | pF |
| Ducy(HXTAL) (2) | Duty cycle | — | 40 | — | 60 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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GD32F470xx Datasheet **Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fLXTAL(1) | Crystal or ceramic  frequency | VDD = 3.3 V | — | 32.768 | — | kHz |
| CLXTAL(2) (3) | Recommended matching capacitance on OSC32IN  and OSC32OUT | — | — | 15 | — | pF |
| Ducy(LXTAL)(2) | Crystal or ceramic duty  cycle | — | 30 | — | 70 | % |
| gm(2) | Oscillator transconductance | Medium low driving  capability | — | 6 | — | μA/V |
| Higher driving  capability | — | 18 | — |
| IDDLXTAL (1) | Crystal or ceramic operating  current | LXTALDRI= 0 | — | 0.8 | — | μA |
| LXTALDRI= 1 | — | 1.6 | — |
| tSULXTAL(1) (4) | Crystal or ceramic startup  time | LXTALDRI= 0 | — | 369 | — | ms |
| LXTALDRI= 1 | — | 175 | — | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) CLXTAL1 = CLXTAL2 = 2\*(CLOAD - CS), For CLXTAL1 and CLXTAL2, it is recommended matching capacitance on OSC32IN

and OSC32OUT. For CLOAD, it is crystal/ceramic load capacitance, provided by the crystal or ceramic

manufacturer. For CS, it is PCB and MCU pin stray capacitance.

(4) tSULXTAL is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator

stabilization flags is SET. This value varies significantly with the crystal manufacturer.

**Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fLXTAL\_ext(1) | External clock source or oscillator  frequency | VDD = 3.3 V | — | 32.768 | 1000 | kHz |
| VLXTALH(2) | OSC32IN input pin high level voltage | — | 0.7  VDD | — | VDD | V |
| VLXTALL(2) | OSC32IN input pin low level voltage | — | VSS | — | 0.3 VDD |
| tH/L(LXTAL) (2) | OSC32IN high or low time | — | 450 | — | — | ns |
| tR/F(LXTAL) (2) | OSC32IN rise or fall time | — | — | — | 50 |
| CIN(2) | OSC32IN input capacitance | — | — | 5 | — | pF |
| Ducy(LXTAL)  (2) | Duty cycle | — | 30 | 50 | 70 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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**4.8.**

**Internal clock characteristics**

**Table 4-17. High speed internal clock (IRC16M) characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fIRC16M | High Speed Internal  Oscillator (IRC16M)  frequency | VDD = VDDA = 3.3 V | — | 16 | — | MHz |
| ACCIRC16M | IRC16M oscillator  Frequency accuracy,  Factory-trimmed | VDD = VDDA = 3.3 V,  TA = -40 °C ~ +85 °C for grade  6 devices | — | -1.73 to  1.1 (1) | — | % |
| VDD = VDDA = 3.3 V,  TA = -40 °C ~ +105 °C for  grade 7 devices | — | -1.8 to  1.1 (1) | — |
| VDD = VDDA = 3.3 V, TA = 25 °C | -1.0 | — | +1.0 |
| IRC16M oscillator  Frequency accuracy, User  trimming step(1) | — | — | 0.5 | — | % |
| DucyIRC16M(2) | IRC16M oscillator duty  cycle | VDD = VDDA = 3.3 V | 45 | 50 | 55 | % |
| IDDIRC16M+  IDDAIRC16M(1) | IRC16M oscillator  operating current | VDD = VDDA = 3.3 V,  fHCLK =fHXTAL = 25 MHz | — | 47 | — | μA |
| tSUIRC16M(1) | IRC16M oscillator startup  time | VDD = VDDA = 3.3 V,  fHCLK =fHXTAL\_PLL = 200 MHz | — | 1.18 | — | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

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**Table 4-18. High speed internal clock (IRC48M) characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fIRC48M | High Speed Internal Oscillator (IRC48M)  frequency | VDD = 3.3 V | — | 48 | — | MHz |
| ACCIRC48M | IRC48M oscillator Frequency accuracy,  Factory-trimmed | VDD = VDDA = 3.3 V,  TA = -40 °C ~ +85 °C for  grade 6 devices | — | -1.31 to  0.39 (1) | — | % |
| VDD = VDDA = 3.3 V,  TA = -40 °C ~ +105 °C for  grade 7 devices | — | -1.48 to  0.39 (1) | — |
| VDD = VDDA = 3.3 V,  TA = 25 °C | -2.0 | — | +2.0 |
| IRC48M oscillator  Frequency accuracy, User  trimming step(1) | — | — | 0.12 | — | % |
| DIRC48M(2) | IRC48M oscillator duty  cycle | VDD = VDDA = 3.3 V | 45 | 50 | 55 | % |
| IDDIRC48M+  IDDAIRC48M(1) | IRC48M oscillator  operating current | VDD = VDDA = 3.3 V,  fHCLK = fIRC16M = 16 MHz | — | 358 | — | μA |
| tSUIRC48M(1) | IRC48M oscillator startup  time | VDD = VDDA = 3.3 V,  fHCLK = fHXTAL\_PLL = 200 MHz | — | 1.23 | — | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-19. Low speed internal clock (IRC32K) characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fIRC32K(1) | Low Speed Internal oscillator  (IRC32K) frequency | VDD = VDDA = 3.3 V | — | 32 | — | kHz |
| IDDAIRC32K(2) | IRC32K oscillator operating  current | VDD = VDDA = 3.3 V,  fHCLK = fIRC16M = 16 MHz | — | 0.43 | — | μA |
| tSUIRC32K(2) | IRC32K oscillator startup  time | VDD = VDDA = 3.3 V, fHCLK =  fHXTAL\_PLL = 200 MHz | — | 22.1 | — | μs |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

**4.9.**

**PLL characteristics**

**Table 4-20. PLL characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fPLLIN(1) | PLL input clock frequency | — | 1 | — | 4 | MHz |
| fPLLOUT(2) | PLL output clock frequency | — | 32 | — | 250 | MHz |
| fVCO(2) | PLL VCO output clock  frequency | — | 64 | — | 500 | MHz |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| tLOCK(2) | PLL lock time | — | — | — | 400 | μs |
| IDDA(1)(3) | Current consumption on  VDDA | VCO freq = 400 MHz | — | 797 | — | μA |
| JitterPLL | Cycle to cycle Jitter(rms) | System clock | — | 40 | — | ps |
| Cycle to cycle Jitter  （peak to peak） | — | 400 | — |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) System clock = HXTAL = 25 MHz, PLL clock source = HXTAL/25 = 1 MHz, fPLLOUT = 100 MHz.

(4) Value given with main PLL running.

**Table 4-21. PLLI2S characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fPLLIN(1) | PLLI2S input clock  frequency | — | 1 | — | 4 | MHz |
| fPLLOUT(2) | PLLI2S output clock  frequency | — | 32 | — | 250 | MHz |
| fVCO(2) | PLLI2S VCO output clock  frequency | — | 64 | — | 500 | MHz |
| tLOCK(2) | PLLI2S lock time | — | — | — | 400 | μs |
| IDDA(1)(3) | Current consumption on  VDDA | VCO freq = 400 MHz | — | 814 | — | μA |
| JitterPLL | Cycle to cycle Jitter(rms) | System clock | — | 40 | — | ps |
| Cycle to cycle Jitter  （peak to peak） | — | 400 | — |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) System clock = HXTAL = 25 MHz, PLL clock source = HXTAL/25 = 1 MHz, fPLLOUT = 100 MHz.

(4) Value given with main PLLI2S running.

**Table 4-22. PLLSAI characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fPLLIN(1) | PLLSAI input clock  frequency | — | 1 | — | 4 | MHz |
| fPLLOUT(2) | PLLSAI output clock  frequency | — | 32 | — | 250 | MHz |
| fVCO(2) | PLLSAI VCO output clock  frequency | — | 64 | — | 500 | MHz |
| tLOCK(2) | PLLSAI lock time | — | — | — | 400 | μs |
| IDDA(1)(3) | Current consumption on  VDDA | VCO freq = 400 MHz | — | 796 | — | μA |
| JitterPLL | Cycle to cycle Jitter(rms) | System clock | — | 40 | — | ps |
| Cycle to cycle Jitter  （peak to peak） | — | 400 | — |

(1) Based on characterization, not tested in production.

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(2) Guaranteed by design, not tested in production.

(3) System clock = HXTAL = 25 MHz, PLL clock source = HXTAL/25 = 1 MHz, fPLLOUT = 100 MHz.

(4) Value given with main PLLSAI running.

**Table 4-23. PLL spread spectrum clock generation (SSCG) characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| FMOD | Modulation frequency | — | — | — | 10 | KHz |
| Mdamp | Peak modulation amplitude | — | — | — | 2 | % |
| MODCNT\*  MODSTEP | — | — | — | — | 215-1 | — |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

***Equation 1***: SSCG configuration equation:

MODCNT = round(fPLLIN/4/fmod)

MODSTEP = round(mdamp ∗ PLLN ∗ 214/(MODCNT ∗ 100)) The formula above ([Equation](#PageMark91) [1](#PageMark91)) is SSCG configuration equation.

**4.10.**

**Memory characteristics**

**Table 4-24. Flash memory characteristics(1)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min**(1) | **Typ**(1) | **Max**(1) | **Unit** |
| PECYC | Number of guaranteed  program /erase cycles before  failure (Endurance) | — | 100 | — | — | kcycles |
| tREAD | Read time at code flash area | — | 1 | — | hclks |
| Read time at data flash area | 56 | — | 4176 |
| tRET | Data retention time | — | — | 20 | — | years |
| tPROG | Word programming time | TA range(2) | — | 37.5 | 180 | μs |
| tERASE4kB | Page(4kB) erase time | — | 45 | — | ms |
| tERASE16kB | Sector(16kB) erase time | — | 200 | 2000 |
| tERASE64kB | Sector(64kB) erase time | — | 300 | 4000 |
| tERASE128kB | Sector(128kB) erase time | — | 600 | 8000 |
| tMERASE(512K) | Mass erase time | — | 2.4 | 32 | s |
| tMERASE(1MB) | Mass erase time | — | 4.8 | 64 | s |
| tMERASE(2MB) | Mass erase time | — | 9.6 | 128 | s |
| tMERASE(3MB) | Mass erase time | — | 14.4 | 192 | s |

(1) Guaranteed by design and/or characterization, not 100% tested in production.

(2) For grade 6 devices, TA range= -40°C ~ +85°C. For grade 7 devices, TA range= -40°C ~ +105°C.

**4.11.**

**NRST pin characteristics**

**Table 4-25. NRST pin characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| VIL(NRST)(1) | NRST Input low level voltage | VDD = VDDA = 2.6 V | -0.3 | — | 0.3 VDD | V |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| VIH(NRST)(1) | NRST Input high level voltage |  | 0.7 VDD | — | VDD + 0.3 |  |
| Vhyst(1) | Schmidt trigger Voltage hysteresis | — | 440 | — | mV |
| VIL(NRST)(1) | NRST Input low level voltage | VDD = VDDA = 3.3 V | -0.3 | — | 0.3 VDD | V |
| VIH(NRST)(1) | NRST Input high level voltage | 0.7 VDD | — | VDD + 0.3 |
| Vhyst(1) | Schmidt trigger Voltage hysteresis | — | 490 | — | mV |
| VIL(NRST)(1) | NRST Input low level voltage | VDD = VDDA = 3.6 V | -0.3 | — | 0.3 VDD | V |
| VIH(NRST)(1) | NRST Input high level voltage | 0.7 VDD | — | VDD + 0.3 |
| Vhyst(1) | Schmidt trigger Voltage hysteresis | — | 510 | — | mV |
| Rpu(2) | Pull-up equivalent resistor | — | — | 40 | — | kΩ |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Figure 4-5. Recommended external NRST pin circuit(1)**

**VDD** **VDD**

External reset circuit 10 kΩ RPU

**NRST**

K 100 nF

GND

(1) Unless the voltage on NRST pin go below VIL(NRST) level, the device would not generate a reliable reset.

**4.12.**

**GPIO characteristics**

**Table 4-26. I/O port DC characteristics(1)(3)**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| VIL | Standard IO Low level  input voltage | | 2.6 V ≤VDD = VDDA ≤ 3.6 V | — | — | 0.3 VDD | V |
| 5V-tolerant IO Low level  input voltage | | 2.6 V ≤VDD = VDDA ≤ 3.6 V | — | — | 0.3 VDD | V |
| VIH | Standard IO High level  input voltage | | 2.6 V ≤VDD = VDDA ≤ 3.6 V | 0.7 VDD | — | — | V |
| 5V-tolerant IO High  level input voltage | | 2.6 V ≤VDD = VDDA ≤ 3.6 V | 0.7 VDD | — | — | V |
| RPU(2) | Internal pull-  up resistor | All pins | VIN = VSS | — | 40 | — | kΩ |
| PA10 | — | — | 10 | — |
| RPD(2) | Internal pull-  down resistor | All pins | VIN = VDD | — | 40 | — | kΩ |
| PA10 | — | — | 10 | — |

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|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |  |
| **IO\_Speed:level 3** | | | | | | |
| VOL | Low level output voltage for an IO Pin  (IIO = +8 mA) | VDD = 2.6 V | — | — | 0.2 | V |
| VDD = 3.3 V | — | — | 0.2 |
| VDD = 3.6 V | — | — | 0.2 |
| Low level output voltage for an IO Pin  (IIO = +20 mA) | VDD = 2.6 V | — | — | 0.29 |
| VDD = 3.3 V | — | — | 0.27 |
| VDD = 3.6 V | — | — | 0.26 |
| VOH | High level output voltage for an IO Pin  (IIO = +8 mA) | VDD = 2.6 V | 2.38 | — | — |
| VDD = 3.3 V | 3.1 | — | — |
| VDD = 3.6 V | 3.4 | — | — |
| High level output voltage for an IO Pin  (IIO = +20 mA) | VDD = 2.6 V | 2.22 | — | — |
| VDD = 3.3 V | 2.98 | — | — |
| VDD = 3.6 V | 3.29 | — | — |
| **IO\_Speed:level 2** | | | | | | |
| VOL | Low level output voltage for an IO Pin  (IIO = +8 mA) | VDD = 2.6 V | — | — | 0.25 | V |
| VDD = 3.3 V | — | — | 0.24 |
| VDD = 3.6 V | — | — | 0.24 |
| Low level output voltage for an IO Pin  (IIO = +20 mA) | VDD = 2.6 V | — | — | 0.43 |
| VDD = 3.3 V | — | — | 0.37 |
| VDD = 3.6 V | — | — | 0.36 |
| VOH | High level output voltage for an IO Pin  (IIO = +8 mA) | VDD = 2.6 V | 2.32 | — | — |
| VDD = 3.3 V | 3.04 | — | — |
| VDD = 3.6 V | 3.36 | — | — |
| High level output voltage for an IO Pin  (IIO = +20 mA) | VDD = 2.6 V | 2.05 | — | — |
| VDD = 3.3 V | 2.84 | — | — |
| VDD = 3.6 V | 3.17 | — | — |
| **IO\_Speed:level 1** | | | | | | |
| VOL | Low level output voltage for an IO Pin  (IIO = +8 mA) | VDD = 2.6 V | — | — | 0.37 | V |
| VDD = 3.3 V | — | — | 0.38 |
| VDD = 3.6 V | — | — | 0.34 |
| (IIO = +15 mA) | VDD = 2.6 V | — | — | 0.57 |
| Low level output voltage for an IO Pin  (IIO = +20 mA) | VDD = 3.3 V | — | — | 0.66 |
| VDD = 3.6 V | — | — | 0.64 |
| VOH | High level output voltage for an IO Pin  (IIO = +8 mA) | VDD = 2.6 V | 2.15 | — | — |
| VDD = 3.3 V | 2.92 | — | — |
| VDD = 3.6 V | 3.23 | — | — |
| (IIO = +15 mA) | VDD = 2.6 V | 1.83 | — | — |
| High level output voltage for an IO Pin  (IIO = +20 mA) | VDD = 3.3 V | 2.45 | — | — |
| VDD = 3.6 V | 2.81 | — | — |

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|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |  |
| **IO\_Speed:level 0** | | | | | | |
| VOL | Low level output voltage for an IO Pin  (IIO = +1 mA) | VDD = 2.6 V | — | — | 0.17 | V |
| VDD = 3.3 V | — | — | 0.15 |
| VDD = 3.6 V | — | — | 0.15 |
| Low level output voltage for an IO Pin  (IIO = +4 mA) | VDD = 2.6 V | — | — | 0.80 |
| VDD = 3.3 V | — | — | 0.63 |
| VDD = 3.6 V | — | — | 0.60 |
| VOH | High level output voltage for an IO Pin  (IIO = +1 mA) | VDD = 2.6 V | 2.38 | — | — |
| VDD = 3.3 V | 3.12 | — | — |
| VDD = 3.6 V | 3.42 | — | — |
| High level output voltage for an IO Pin  (IIO = +4 mA) | VDD = 2.6 V | 1.45 | — | — |
| VDD = 3.3 V | 2.48 | — | — |
| VDD = 3.6 V | 2.83 | — | — |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) All pins except PC13 / PC14 / PC15 / PI8. Since PC13 to PC15 and PI8 are supplied through the Power Switch,

which can only be obtained by a small current( typical source capability:3mA shared between these IOs, but sink capability is same as other IO) , the speed of GPIOs PC13 to PC15 and PI8 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).

**Table 4-27. I/O port AC characteristics(1)(2)(4)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **GPIOx\_OSPD[1:0] bit value(3)** | **Parameter** | **Conditions** | **Max** | **Unit** |
| GPIOx\_OSPD0->OSPDy[1:0] = 00  （IO\_Speed:level 0） | TRise/TFall | 2.6 ≤ VDD ≤ 3.6 V, CL = 10 pF | 51 | ns |
| 2.6 ≤VDD≤ 3.6 V, CL = 30 pF | 63.2 |
| 2.6 ≤VDD≤ 3.6 V, CL = 50 pF | 74.2 |
| GPIOx\_OSPD0->OSPDy[1:0] = 01  （IO\_Speed:level 1） | TRise/TFall | 2.6 ≤ VDD ≤ 3.6 V, CL = 10 pF | 3.6 | ns |
| 2.6 ≤VDD≤ 3.6 V, CL = 30 pF | 9.6 |
| 2.6 ≤VDD≤ 3.6 V, CL = 50 pF | 12.2 |
| GPIOx\_OSPD0->OSPDy[1:0] = 10  （IO\_Speed: level 2） | TRise/TFall | 2.6 ≤ VDD ≤ 3.6 V, CL = 10 pF | 2.2 | ns |
| 2.6 ≤VDD≤ 3.6 V, CL = 30 pF | 3 |
| 2.6 ≤VDD≤ 3.6 V, CL = 50 pF | 3.8 |
| GPIOx\_OSPD0->OSPDy[1:0] = 11  （IO\_Speed:level 3） | TRise/TFall | 2.6 ≤ VDD ≤ 3.6 V, CL = 10 pF | 2 | ns |
| 2.6 ≤VDD≤ 3.6 V, CL = 30 pF | 2.8 |
| 2.6 ≤VDD≤ 3.6 V, CL = 50 pF | 3.4 |

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all test results given for TA = 25 °C.

(3) The I/O speed is configured using the GPIOx\_OSPD -> OSPDy[1:0]bits.

(4) Only for reference, Depending on user’s design.

(5) Max frequency is defined when the sum of rise time plus the fall time is less than 2/3 cycle.

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**4.13.**

**ADC characteristics**

**Table 4-28. ADC characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| VDDA(1) | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| VIN(1) | ADC input voltage range | — | 0 | — | VREFP | V |
| VREFP(2)(3) | Positive Reference Voltage | — | 2.6 | — | VDDA | V |
| VREFN(2) | Negative Reference Voltage | — | — | VSSA | — | V |
| fADC(1) | ADC clock | — | 0.1 | — | 40 | MHz |
| fS(1) | Sampling rate | 12-bit | 0.007 | — | 2.6 | MSP  S |
| 10-bit | 0.008 | — | 3.1 |
| 8-bit | 0.01 | — | 3.6 |
| 6-bit | 0.011 | — | 4.4 |
| VAIN(1) | Analog input voltage | 16 external; 3 internal | 0 | — | VREFP | V |
| RAIN(2) | External input impedance | See ***Equation 2*** | — | — | 308.6 | kΩ |
| RADC(2) | Input sampling switch  resistance | — | — | — | 0.55 | kΩ |
| CADC(2) | Input sampling capacitance | No pin/pad capacitance  included | — | — | 4.0 | pF |
| tCAL(2) | Calibration time | fADC = 40 MHz | — | 3.275 | — | μs |
| ts(2) | Sampling time | fADC = 40 MHz | 0.075 | — | 12 | μs |
| tCONV(2) | Total conversion time (including  sampling time) | 12-bit | — | 15 | — | 1/ fADC |
| 10-bit | — | 13 | — |
| 8-bit | — | 11 | — |
| 6-bit | — | 9 | — |
| tSU(2) | Startup time | — | — | — | 1 | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) VREFP should always be equal to or less than VDDA, especially during power up.

***Equation 2****:* RAIN max formula RAIN <

Ts fADC∗CADC∗ln(2N+2) − RADC

The formula above ([Equation](#PageMark95) [2](#PageMark95)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 4-29. ADC RAIN max for fADC = 40 MHz(2)**

|  |  |  |
| --- | --- | --- |
| **Ts (cycles)** | **ts (us)** | **RAIN max (KΩ)** |
| 3 | 0.075 | 1.3 |
| 15 | 0.375 | 9.1 |
| 28 | 0.7 | 17.4 |
| 55 | 1.375 | 34.8 |
| 84 | 2.1 | 53.5 |
| 112 | 2.8 | 71.5 |
| 144 | 3.6 | 92.4 |

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|  |  |  |  |
| --- | --- | --- | --- |
|  | **Ts (cycles)** | **ts (us)** | **RAIN max (KΩ)** |
| 480 | 12 | 308.6 |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**Table 4-30. ADC dynamic accuracy at fADC = 40 MHz(1)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Test conditions** | **Min** | **Typ** | **Max** | **Unit** |
| ENOB | Effective number of bits | fADC = 40 MHz  VDDA = VREFP = 3.3 V  Input Frequency = 110  kHz  Temperature = 25 ℃ | — | 10.9 | — | bits |
| SNDR | Signal-to-noise and distortion ratio | — | 67.3 | — | dB |
| SNR | Signal-to-noise ratio | — | 67.7 | — |
| THD | Total harmonic distortion | — | -75 | — |

(1) Based on characterization, not tested in production.

**Table 4-31. ADC static accuracy at fADC = 40 MHz(1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Test conditions** | **Typ** | **Max** | **Unit** |
| Offset | Offset error | fADC = 40 MHz VDDA = VREFP = 3.3 V | ±1 | — | LSB |
| DNL | Differential linearity error | ±1 | — |
| INL | Integral linearity error | ±1.5 | — |

(1) Based on characterization, not tested in production.

**4.14.**

**Temperature sensor characteristics**

**Table 4-32. Temperature sensor characteristics(1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** |
| TL | VSENSE linearity with temperature | — | ±1.5 | — | ℃ |
| Avg\_Slope | Average slope | — | 4.4 | — | mV/℃ |
| V25 | Voltage at 25 °C | — | 1.4 | — | V |
| tS\_temp (2) | ADC sampling time when reading the temperature | — | 17.1 | — | μs |

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

**4.15.**

**DAC characteristics**

**Table 4-33. DAC characteristics**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| VDDA(1) | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| VREFP(2) | Positive Reference Voltage | — | 2.6 | — | VDDA | V |
| VREFN(2) | Negative Reference  Voltage | — | — | VSSA | — | V |
| RLOAD(2) | Resistive load | Resistive load with buffer ON | 5 | — | — | kΩ |
| Ro(2) | Impedance output | Impedance output with buffer  OFF | — | — | 15 | kΩ |
| CLOAD(2) | Capacitive load | Capacitive load with buffer ON | — | — | 50 | pF |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| DAC\_OUT  min(2) | Lower DAC\_OUT voltage | Lower DAC\_OUT voltage with  buffer ON | 0.2 | — | — | V |
| Lower DAC\_OUT voltage with  buffer OFF | 0.5 | — | — | mV |
| DAC\_OUT  max (2) | Higher DAC\_OUT voltage | Higher DAC\_OUT voltage with  buffer ON | — | — | VDDA -  0.2 | V |
| Higher DAC\_OUT voltage with  buffer OFF | — | — | VDDA -  1LSB | V |
| IDDA(1) | DAC current consumption  in quiescent mode | With no load, middle code(0x800) on the input,  VREFP = 3.6 V | — | 350 | — | μA |
| With no load, worst  code(0xF1C) on the input,  VREFP = 3.6 V | — | 430 | — |
| IDDVREFP(1) | DAC current consumption  in quiescent mode | With no load, middle code(0x800) on the input,  VREFP = 3.6 V | — | 115 | — | μA |
| With no load, worst  code(0xF1C) on the input,  VREFP = 3.6 V | — | 298 | — |
| DNL(1) | Differential non linearity | 10-bit configuration | — | — | ±0.75 | LSB |
| 12-bit configuration | — | — | ±3 |
| INL(1) | Integral non linearity | 10-bit configuration | — | — | ±1.25 | LSB |
| 12-bit configuration | — | — | ±5 |
| Offset(1) | Offset error | DAC in 12-bit mode | — | — | ±24 | LSB |
| GE(1) | Gain error | DAC in 12-bit mode | — | — | ±1.5 | % |
| Tsetting(1) | Settling time | CLOAD ≤ 50 pF, RLOAD ≥ 5 kΩ | — | 0.5 | 1 | μs |
| Twakeup(2) | Wakeup from off state | — | — | 5 | 10 | μs |
| Update  rate(2) | Max frequency for a correct  DAC\_OUT change from  code i to i±1LSB | CLOAD ≤ 50 pF, RLOAD ≥ 5 kΩ | — | — | 4 | MS/s |
| PSRR(2) | Power supply rejection  ratio(to VDDA) | No RLoad, CLOAD=50 pF | — | -90 | — | dB |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

**4.16.**

**I2C characteristics**

**Table 4-34. I2C characteristics(1)(2)**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Standard mode** | | **Fast mode** | | **Unit** |
| **Min** | **Max** | **Min** | **Max** |
| tSCL(H) | SCL clock high time | — | 4.0 | — | 0.6 | — | μs |

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|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Conditions** | **Standard mode** | | **Fast mode** | | **Unit** |  |
| **Min** | **Max** | **Min** | **Max** |
| tSCL(L) | SCL clock low time | — | 4.7 | — | 1.3 | — | μs |
| tSU(SDA) | SDA setup time | — | 250 | — | 100 | — | ns |
| th(SDA) | SDA data hold time | — | 0(3) | 3450 | 0 | 900 | ns |
| tr(SDA/SCL) | SDA and SCL rise time | — | — | 1000 | — | 300 | ns |
| tf(SDA/SCL) | SDA and SCL fall time | — | — | 300 | — | 300 | ns |
| th(STA) | Start condition hold time | — | 4.0 | — | 0.6 | — | μs |
| tSU(STA) | Repeated Start condition setup  time | — | 4.7 | — | 0.6 | — | μs |
| tSU(STO) | Stop condition setup time | — | 4.0 | — | 0.6 | — | μs |
| tbuff | Stop to Start condition time (bus  free) | — | 4.7 | — | 1.3 | — | μs |

(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency, fPCLK1 must be at least 2 MHz. To ensure the fast mode I2C

frequency, fPCLK1 must be at least 4 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the

falling edge of SCL.

**Figure 4-6. I2C bus timing diagram**

70%

tSU(STA)

SDA 70% 70% 70%

30% 30% tBUFF

tF(SDA) tR(SDA) tH(SDA)

SCL

tH(STA)

70%

tSCL(H)

tSU(SDA)

70%

30%

tSCL(L) tR(SCL) tF(SCL) tSU(STO)

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**4.17.**

**SPI characteristics**

**Table 4-35. Standard SPI characteristics(1)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fSCK | SCK clock frequency | — | — | — | 30 | MHz |
| tSCK(H) | SCK clock high time | Master mode, fPCLKx = 120 MHz,  presc = 4 | 14.67 | 16.67 | 18.67 | ns |
| tSCK(L) | SCK clock low time | Master mode, fPCLKx = 120 MHz,  presc = 4 | 14.67 | 16.67 | 18.67 | ns |
| **SPI master mode** | | | | | | |
| tV(MO) | Data output valid time | — | — | — | 8 | ns |
| tSU(MI) | Data input setup time | — | 6 | — | — | ns |
| tH(MI) | Data input hold time | — | 0 | — | — | ns |
| **SPI slave mode** | | | | | | |
| tSU(NSS) | NSS enable setup time | — | 0 | — | — | ns |
| tH(NSS) | NSS enable hold time | — | 3.3 | — | — | ns |
| tA(SO) | Data output access time | — | — | 9 | — | ns |
| tDIS(SO) | Data output disable time | — | — | 10 | — | ns |
| tV(SO) | Data output valid time | — | — | 11 | — | ns |
| tSU(SI) | Data input setup time | — | 0 | — | — | ns |
| tH(SI) | Data input hold time | — | 2.2 | — | — | ns |

(1) Based on characterization, not tested in production.

**Figure 4-7. SPI timing diagram - master mode**

tSCK

SCK (CKPH=0 CKPL=0) SCK (CKPH=0 CKPL=1)

SCK (CKPH=1 CKPL=0)

SCK (CKPH=1 CKPL=1)

tSCK(H) tSCK(L)

tSU(MI)

MISO D[0] D[7]

LF=1,FF16=0 tH(MI)

MOSI D[0] D[7]

tV(MO) tH(MO)

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**Figure 4-8. SPI timing diagram - slave mode**

NSS

tSU(NSS) tSCK tH(NSS)

SCK (CKPH=0 CKPL=0) SCK (CKPH=0 CKPL=1)

tSCK(H) tSCK(L)

tH(SO)

tA(SO) tV(SO) tDIS(SO)

MISO D[0] D[7]

tSU(SI)

MOSI

D[0]

tH(SI)

D[7]

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**4.18.**

**I2S characteristics**

**Table 4-36. I2S characteristics(1)(2)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fCK | Clock frequency | Master mode (data: 32 bits,  Audio frequency = 96 kHz) | — | 6.25 | — | MHz |
| Slave mode | — | — | 12.5 |
| tH | Clock high time | — | — | 80 | — | ns |
| tL | Clock low time | — | 80 | — | ns |
| tV(WS) | WS valid time | Master mode | — | 3 | — | ns |
| tH(WS) | WS hold time | Master mode | — | 3 | — | ns |
| tSU(WS) | WS setup time | Slave mode | 0 | — | — | ns |
| tH(WS) | WS hold time | Slave mode | 3 | — | — | ns |
| Ducy(SCK) | I2S slave input clock duty  cycle | Slave mode | — | 50 | — | % |
| tSU(SD\_MR) | Data input setup time | Master mode | 0 | — | — | ns |
| tsu(SD\_SR) | Data input setup time | Slave mode | 0 | — | — | ns |
| tH(SD\_MR) | Data input hold time | Master receiver | 1 | — | — | ns |
| tH(SD\_SR) | Slave receiver | 3 | — | — | ns |
| tV(SD\_ST) | Data output valid time | Slave transmitter  (after enable edge) | — | — | 9 | ns |
| tH(SD\_ST) | Data output hold time | Slave transmitter  (after enable edge) | 6 | — | — | ns |
| tV(SD\_MT) | Data output valid time | Master transmitter  (after enable edge) | — | — | 6 | ns |
| tH(SD\_MT) | Data output hold time | Master transmitter  (after enable edge) | 0 | — | — | ns |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

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**Figure 4-9. I2S timing diagram - master mode**

tCK

CPOL=0

CPOL=1

tL

WS output tV(WS) tH tH(WS)

tV(SD\_MT) tH(SD\_MT)

SD transmit

SD receive

D[0]

D[0]

tSU(SD\_MR)

tH(SD\_MR)

**Figure 4-10. I2S timing diagram - slave mode**

tCK

CPOL=0

tL

CPOL=1

tH

WS input

tH(WS)

tSU(WS) tV(SD\_ST) tH(SD\_ST)

SD transmit

SD receive

D[0]

D[0]

tSU(SD\_SR)

tH(SD\_SR)

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**4.19.**

**USART characteristics**

**Table 4-37. USART characteristics(1)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fSCK | SCK clock frequency | fPCLKx = 120 MHz | — | — | 60 | MHz |
| tSCK(H) | SCK clock high time | fPCLKx = 120 MHz | 8.33 | — | — | ns |
| tSCK(L) | SCK clock low time | fPCLKx = 120 MHz | 8.33 | — | — | ns |

(1) Guaranteed by design, not tested in production.

**4.20.**

**SDIO characteristics**

**Table 4-38. SDIO characteristics(1)(2)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fPP(3) | Clock frequency in data transfer mode | — | 0 | — | 48 | MHz |
| tW(CKL) (3) | Clock low time | fpp = 48 MHz | 9.5 | 10.5 | — | ns |
| tW(CKH) (3) | Clock high time | fpp = 48 MHz | 9.3 | 10.3 | — | ns |
| CMD, D inputs (referenced to CK) in MMC and SD HS mode | | | | | | |
| tISU(4) | Input setup time HS | fpp = 48 MHz | 4 | — | — | ns |
| tIH(4) | Input hold time HS | fpp = 48 MHz | 3 | — | — | ns |
| CMD, D outputs (referenced to CK) in MMC and SD HS mode | | | | | | |
| tOV(3) | Output valid time HS | fpp = 48 MHz | — | — | 13.8 | ns |
| tOH(3) | Output hold time HS | fpp = 48 MHz | 12 | — | — | ns |
| CMD, D inputs (referenced to CK) in SD default mode | | | | | | |
| tISUD(4) | Input setup time SD | fpp = 24 MHz | 3 | — | — | ns |
| tIHD(4) | Input hold time SD | fpp = 24 MHz | 3 | — | — | ns |
| CMD, D outputs (referenced to CK) in SD default mode | | | | | | |
| tOVD(3) | Output valid default time SD | fpp = 24 MHz | — | 2.4 | 2.8 | ns |
| tOHD(3) | Output hold default time SD | fpp = 24 MHz | 2 | — | — | ns |

(1) CLK timing is measured at 50% of VDD.

(2) Capacitive load CL = 30 pF.

(3) Based on characterization, not tested in production.

(4) Guaranteed by design, not tested in production.

**4.21.**

**CAN characteristics**

Refer to [***Table***](#PageMark92)[***4-26.***](#PageMark92)[***I/O***](#PageMark92)[***port***](#PageMark92)[***DC***](#PageMark92)[***characteristics(1)***](#PageMark92)for more details on the input/output alternate function characteristics (CANTX and CANRX).

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**4.22.**

**USBFS characteristics**

**Table 4-39. USBFS start up time**

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Max** | **Unit** |
| tSTARTUP(1) | USBFS startup time | 1 | μs |

(1) Guaranteed by design, not tested in production.

**Table 4-40. USBFS DC electrical characteristics**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| Input  levels(1) | VDD | USBFS operating voltage | — | 3 | — | 3.6 | V |
| VDI | Differential input sensitivity | — | 0.2 | — | — |
| VCM | Differential common mode range | Includes VDI range | 0.8 | — | 2.5 |
| VSE | Single ended receiver threshold | — | 1.3 | — | 2.0 |
| Output  levels (2) | VOL | Static output level low | RL of 1.0 kΩ to 3.6 V | — | 0.06 | 0.3 | V |
| VOH | Static output level high | RL of 15 kΩ to VSS | 2.8 | 3.3 | 3.6 |
| RPD(2) | | PA11, PA12(USBFS\_DM/DP)  PB14, PB15(USBHS\_ DM/DP) | VIN = VDD | 17 | 21 | 25 | kΩ |
| PA9(USBFS\_VBUS)  PB13(USBHS\_VBUS) | 0.72 | 0.9 | 1.1 |
| RPU(2) | | PA11, PA12(USBFS\_DM/DP)  PB14, PB15(USBHS\_ DM/DP) | VIN = VSS | 1.2 | 1.5 | 1.8 |
| PA9(USBFS\_VBUS)  PB13(USBHS\_VBUS) | 0.24 | 0.3 | 0.33 |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

**Table 4-41. USBFS full speed-electrical characteristics(1)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| tR | Rise time | CL = 50 pF | 4 | — | 20 | ns |
| tF | Fall time | CL = 50 pF | 4 | — | 20 | ns |
| tRFM | Rise/ fall time matching | tR / tF | 90 | — | 110 | % |
| vCRS | Output signal crossover voltage | — | 1.3 | — | 2.0 | V |

(1) Guaranteed by design, not tested in production.

**Figure 4-11. USBFS timings: definition of data signal rise and fall time**

Crossover

points

Differential

data lines VCRS

VSS

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**4.23.** **USBHS characteristics**

**(1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** |
| VDD | USBHS operating voltage | 3.0 | — | 3.6 | V |
| fHCLK | fHCLK value to guarantee proper  operation of USBHS interface | 30 | — | — | MHz |
| FSTART\_8BIT | Frequency (first transition) 8-bit ± 10% | 54 | 60 | 66 | MHz |
| FSTEADY | Frequency (steady state) ±500 ppm | 59.97 | 60 | 60.63 | MHz |
| DSTART\_8BIT | Duty cycle (first transition) 8-bit ± 10% | 40 | 50 | 60 | % |
| DSTEADY | Duty cycle (steady state) ±500 ppm | 49.975 | 50 | 50.025 | % |

(1) Guaranteed by design, not tested in production.

**Table 4-43. USB-ULPI Dynammic characteristics**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** |
| tSC | Control in (ULPI\_DIR, ULPI\_NXT) setup time | — | — | 2 | ns |
| tHC | Control in (ULPI\_DIR, ULPI\_NXT) hold time | 0.5 | — | — | ns |
| tSD | Data in setup time | — | — | 2 | ns |
| tHD | Data in hold time | 0 | — | — | ns |

(1) Guaranteed by design, not tested in production.

**4.24.**

**Ethernet (ENET) characteristics**

**Table 4-44. Dynamics characteristics: Ethernet MAC signals for SMI(1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** |
| tMDC | MDC cycle time(2.38 MHz) | 411 | 420 | 425 | ns |
| TD(MDIO） | Write data valid delay time | 1/4  tmdc | 1/4  tmdc | 1/4  tmdc |
| tSU(MDIO) | Read data setup time | 12 | — | — |
| tH(SD\_MR) | Read data hold time | 0 | — | — |

(1) Guaranteed by design, not tested in production.

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**Figure 4-12. Ethernet SMI timing diagram**

tMDC

ETH\_MDC TD

Th(MDIOI)

ETH\_MDIO(O)

ETH\_MDIO(I)

**4.25.**

**EXMC characteristics**

**Table 4-45. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)(3)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| tw(NE) | EXMC\_NE low time | 19.85 | 21.85 | ns |
| tV(NOE\_NE) | EXMC\_NEx low to EXMC\_NOE low | 0 | — | ns |
| tw(NOE) | EXMC\_NOE low time | 19.85 | 21.85 | ns |
| th(NE\_NOE) | EXMC\_NOE high to EXMC\_NE high hold time | 0 | — | ns |
| tv(A\_NE) | EXMC\_NEx low to EXMC\_A valid | 0 | — | ns |
| tv(BL\_NE) | EXMC\_NEx low to EXMC\_BL valid | 0 | — | ns |
| tsu(DATA\_NE) | Data to EXMC\_NEx high setup time | 15.68 | — | ns |
| tsu(DATA\_NOE) | Data to EXMC\_NOEx high setup time | 15.68 | — | ns |
| th(DATA\_NOE) | Data hold time after EXMC\_NOE high | 0 | — | ns |
| th(DATA\_NE) | Data hold time after EXMC\_NEx high | 0 | — | ns |
| tv(NADV\_NE) | EXMC\_NEx low to EXMC\_NADV low | 0 | — | ns |
| tw(NADV) | EXMC\_NADV low time | 3.17 | 5.17 | ns |

(1) CL = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: fHCLK = 240 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

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**Table 4-46. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)(3)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| tw(NE) | EXMC\_NE low time | 11.51 | 13.51 | ns |
| tV(NWE\_NE) | EXMC\_NEx low to EXMC\_NWE low | 3.17 | — | ns |
| tw(NWE) | EXMC\_NWE low time | 3.17 | 5.17 | ns |
| th(NE\_NWE) | EXMC\_NWE high to EXMC\_NE high hold time | 3.17 | 5.17 | ns |
| tv(A\_NE) | EXMC\_NEx low to EXMC\_A valid | 0 | — | ns |
| tV(NADV\_NE) | EXMC\_NEx low to EXMC\_NADV low | 0 | — | ns |
| tw(NADV) | EXMC\_NADV low time | 3.17 | 5.17 | ns |
| th(AD\_NADV) | EXMC\_AD(address) valid hold time after  EXMC\_NADV high | 7.34 | — | ns |
| th(A\_NWE) | Address hold time after EXMC\_NWE high | 3.17 | — | ns |
| th(BL\_NWE) | EXMC\_BL hold time after EXMC\_NWE high | 3.17 | — | ns |
| tv(BL\_NE) | EXMC\_NEx low to EXMC\_BL valid | 0 | — | ns |
| tv(DATA\_NADV) | EXMC\_NADV high to DATA valid | 0 | — | ns |
| th(DATA\_NWE) | Data hold time after EXMC\_NWE high | 3.17 | — | ns |

(1) CL = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: fHCLK = 240 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

**Table 4-47. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| tw(NE) | EXMC\_NE low time | 28.19 | 30.19 | ns |
| tV(NOE\_NE) | EXMC\_NEx low to EXMC\_NOE low | 11.51 | — | ns |
| tw(NOE) | EXMC\_NOE low time | 15.68 | 17.68 | ns |
| th(NE\_NOE) | EXMC\_NOE high to EXMC\_NE high hold time | 0 | — | ns |
| tv(A\_NE) | EXMC\_NEx low to EXMC\_A valid | 0 | — | ns |
| tv(A\_NOE) | Address hold time after EXMC\_NOE high | 0 | — | ns |
| tv(BL\_NE) | EXMC\_NEx low to EXMC\_BL valid | 0 | — | ns |
| th(BL\_NOE) | EXMC\_BL hold time after EXMC\_NOE high | 0 | — | ns |
| tsu(DATA\_NE) | Data to EXMC\_NEx high setup time | 15.68 | — | ns |
| tsu(DATA\_NOE) | Data to EXMC\_NOEx high setup time | 15.68 | — | ns |
| th(DATA\_NOE) | Data hold time after EXMC\_NOE high | 0 | — | ns |
| th(DATA\_NE) | Data hold time after EXMC\_NEx high | 0 | — | ns |
| tv(NADV\_NE) | EXMC\_NEx low to EXMC\_NADV low | 0 | — | ns |
| tw(NADV) | EXMC\_NADV low time | 3.17 | 5.17 | ns |
| Th(AD\_NADV) | EXMC\_AD(adress) valid hold time after  EXMC\_NADV high | 3.17 | 5.17 | ns |

(1) CL = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: fHCLK= 240 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

**Table 4-48. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| tw(NE) | EXMC\_NE low time | 19.85 | 21.85 | ns |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| tV(NWE\_NE) | EXMC\_NEx low to EXMC\_NWE low | 3.17 | — | ns |
| tw(NWE) | EXMC\_NWE low time | 11.51 | 13.51 | ns |
| th(NE\_NWE) | EXMC\_NWE high to EXMC\_NE high hold time | 3.17 | — | ns |
| tv(A\_NE) | EXMC\_NEx low to EXMC\_A valid | 0 | — | ns |
| tV(NADV\_NE) | EXMC\_NEx low to EXMC\_NADV low | 0 | — | ns |
| tw(NADV) | EXMC\_NADV low time | 3.17 | 5.17 | ns |
| th(AD\_NADV) | EXMC\_AD(address) valid hold time after  EXMC\_NADV high | 3.17 | — | ns |
| th(A\_NWE) | Address hold time after EXMC\_NWE high | 3.17 | — | ns |
| th(BL\_NWE) | EXMC\_BL hold time after EXMC\_NWE high | 3.17 | — | ns |
| tv(BL\_NE) | EXMC\_NEx low to EXMC\_BL valid | 0 | — | ns |
| tv(DATA\_NADV) | EXMC\_NADV high to DATA valid | 3.17 | — | ns |
| th(DATA\_NWE) | Data hold time after EXMC\_NWE high | 3.17 | — | ns |

(1) CL = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: fHCLK = 240 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

**Table 4-49. Synchronous multiplexed PSRAM/NOR read timings(1)(2)(3)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| tw(CLK) | EXMC\_CLK period | 16.67 | — | ns |
| td(CLKL-NExL) | EXMC\_CLK low to EXMC\_NEx low | 0 | — | ns |
| td(CLKH-NExH) | EXMC\_CLK high to EXMC\_NEx high | 7.34 | — | ns |
| td(CLKL-NADVL) | EXMC\_CLK low to EXMC\_NADV low | 0 | — | ns |
| td(CLKL-NADVH) | EXMC\_CLK low to EXMC\_NADV high | 0 | — | ns |
| td(CLKL-AV) | EXMC\_CLK low to EXMC\_Ax valid | 0 | — | ns |
| td(CLKH-AIV) | EXMC\_CLK high to EXMC\_Ax invalid | 7.34 | — | ns |
| td(CLKL-NOEL) | EXMC\_CLK low to EXMC\_NOE low | 0 | — | ns |
| td(CLKH-NOEH) | EXMC\_CLK high to EXMC\_NOE high | 7.34 | — | ns |
| td(CLKL-ADV) | EXMC\_CLK low to EXMC\_AD valid | 0 | — | ns |
| td(CLKL-ADIV) | EXMC\_CLK low to EXMC\_AD invalid | 0 | — | ns |

(1) CL = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) (Based on configure: fHCLK = 240 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst =

Enable; CLKDivision = 3 (EXMC\_CLK is 4 divided by HCLK); Data Latency = 1.

**Table 4-50. Synchronous multiplexed PSRAM write timings(1)(2)(3)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| tw(CLK) | EXMC\_CLK period | 16.67 | — | ns |
| td(CLKL-NExL) | EXMC\_CLK low to EXMC\_NEx low | 0 | — | ns |
| td(CLKH-NExH) | EXMC\_CLK high to EXMC\_NEx high | 7.34 | — | ns |
| td(CLKL-NADVL) | EXMC\_CLK low to EXMC\_NADV low | 0 | — | ns |
| td(CLKL-NADVH) | EXMC\_CLK low to EXMC\_NADV high | 0 | — | ns |
| td(CLKL-AV) | EXMC\_CLK low to EXMC\_Ax valid | 0 | — | ns |
| td(CLKH-AIV) | EXMC\_CLK high to EXMC\_Ax invalid | 7.34 | — | ns |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| td(CLKL-NWEL) | EXMC\_CLK low to EXMC\_NWE low | 0 | — | ns |
| td(CLKH-NWEH) | EXMC\_CLK high to EXMC\_NWE high | 7.34 | — | ns |
| td(CLKL-ADIV) | EXMC\_CLK low to EXMC\_AD invalid | 0 | — | ns |
| td(CLKL-DATA) | EXMC\_A/D valid data after EXMC\_CLK low | 0 | — | ns |
| th(CLKL-NBLH) | EXMC\_CLK low to EXMC\_NBL high | 0 | — | ns |

(1) CL = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: fHCLK = 240 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst =

Enable; CLKDivision = 3 (EXMC\_CLK is 4 divided by HCLK); DataLatency = 1.

**Table 4-51. Synchronous non-multiplexed PSRAM/NOR read timings(1)(2)(3)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| tw(CLK) | EXMC\_CLK period | 16.67 | — | ns |
| td(CLKL-NExL) | EXMC\_CLK low to EXMC\_NEx low | 0 | — | ns |
| td(CLKH-NExH) | EXMC\_CLK high to EXMC\_NEx high | 7.34 | — | ns |
| td(CLKL-NADVL) | EXMC\_CLK low to EXMC\_NADV low | 0 | — | ns |
| td(CLKL-NADVH) | EXMC\_CLK low to EXMC\_NADV high | 0 | — | ns |
| td(CLKL-AV) | EXMC\_CLK low to EXMC\_Ax valid | 0 | — | ns |
| td(CLKH-AIV) | EXMC\_CLK high to EXMC\_Ax invalid | 7.34 | — | ns |
| td(CLKL-NOEL) | EXMC\_CLK low to EXMC\_NOE low | 0 | — | ns |
| td(CLKH-NOEH) | EXMC\_CLK high to EXMC\_NOE high | 7.34 | — | ns |

(1) CL = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: fHCLK = 240 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst =

Enable; CLKDivision = 3 (EXMC\_CLK is 4 divided by HCLK); DataLatency = 1.

**Table 4-52. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| tw(CLK) | EXMC\_CLK period | 16.67 | — | ns |
| td(CLKL-NExL) | EXMC\_CLK low to EXMC\_NEx low | 0 | — | ns |
| td(CLKH-NExH) | EXMC\_CLK high to EXMC\_NEx high | 7.34 | — | ns |
| td(CLKL-NADVL) | EXMC\_CLK low to EXMC\_NADV low | 0 | — | ns |
| td(CLKL-NADVH) | EXMC\_CLK low to EXMC\_NADV high | 0 | — | ns |
| td(CLKL-AV) | EXMC\_CLK low to EXMC\_Ax valid | 0 | — | ns |
| td(CLKH-AIV) | EXMC\_CLK high to EXMC\_Ax invalid | 7.34 | — | ns |
| td(CLKL-NWEL) | EXMC\_CLK low to EXMC\_NWE low | 0 | — | ns |
| td(CLKH-NWEH) | EXMC\_CLK high to EXMC\_NWE high | 7.34 | — | ns |
| td(CLKL-DATA) | EXMC\_A/D valid data after EXMC\_CLK low | 0 | — | ns |
| th(CLKL-NBLH) | EXMC\_CLK low to EXMC\_NBL high | 0 | — | ns |

(1) CL = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: fHCLK = 240 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst =

Enable; CLKDivision = 3 (EXMC\_CLK is 4 divided by HCLK); DataLatency = 1.

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**4.26.**

**TIMER characteristics**

**Table 4-53. TIMER characteristics(1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| tres | Timer resolution time | — | 1 | — | tTIMERxCLK |
| fTIMERxCLK = 240 MHz | 4.17 | — | ns |
| fEXT | Timer external clock frequency | — | 0 | fTIMERxCLK/2 | MHz |
| fTIMERxCLK = 240 MHz | 0 | 120 | MHz |
| RES | Timer resolution | TIMERx (except  TIMER1 & TIMER4) | — | 16 | bit |
| TIMER1 & TIMER4 | — | 32 | bit |
| tCOUNTER | 16-bit counter clock period  when internal clock is selected | — | 1 | 65536 | tTIMERxCLK |
| fTIMERxCLK = 240 MHz | 0.004 | 273.07 | μs |
| tMAX\_COUNT | Maximum possible count | — | — | 65536x65536 | tTIMERxCLK |
| fTIMERxCLK = 240 MHz | — | 17.90 | s |

(1) Guaranteed by design, not tested in production.

**4.27.**

**DCI characteristics**

**Table 4-54. DCI characteristics(1)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| Frequency ratio | DCI\_PIXCLK /fHCLK | — | 0.4 |  |
| DCI\_PIXCLK | Pixel clock input | — | 96 | MHz |
| DPixel | Pixel clock input duty cycle | 30 | 70 | % |
| tsu(DATA) | Data input setup time | 2.5 | — | ns |
| th(DATA) | Data input hold time | 1 | — | ns |
| tsu(HSYNC) | DCI\_HS input setup time | 2 | — | ns |
| tsu(VSYNC) | DCI\_VS input setup time | 2 | — | ns |
| th(HSYNC) | DCI\_HS input hold time | 0.5 | — | ns |
| th(VSYNC) | DCI\_VS input hold time | 0.5 | — | ns |

(1) Guaranteed by design, not tested in production.

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**4.28.**

**WDGT characteristics**

**Table 4-55. FWDGT min/max timeout period at 32 kHz (IRC32K)(1)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Prescaler divider** | **PSC[2:0] bits** | **Min timeout RLD[11:0] =**  **0x000** | **Max timeout RLD[11:0]**  **= 0xFFF** | **Unit** |
| 1/4 | 000 | 0.03125 | 511.90625 | ms |
| 1/8 | 001 | 0.03125 | 1023.7812 |
| 1/16 | 010 | 0.03125 | 2047.53125 |
| 1/32 | 011 | 0.03125 | 4095.03125 |
| 1/64 | 100 | 0.03125 | 8190.03125 |
| 1/128 | 101 | 0.03125 | 16380.03125 |
| 1/256 | 110 or 111 | 0.03125 | 32760.03125 |

(1) Guaranteed by design, not tested in production.

**Table 4-56. WWDGT min-max timeout value at 60 MHz (fPCLK1)(1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Prescaler divider** | **PSC[1:0]** | **Min timeout value**  **CNT[6:0] = 0x40** | **Unit** | **Max timeout value**  **CNT[6:0] = 0x7F** | **Unit** |
| 1/1 | 00 | 68.27 | μs | 4.37 | ms |
| 1/2 | 01 | 136.53 | 8.74 |
| 1/4 | 10 | 273.07 | 17.48 |
| 1/8 | 11 | 546.13 | 34.95 |

(1) Guaranteed by design, not tested in production.

**4.29.**

**Parameter conditions**

Unless otherwise specified, all values given for VDD = VDDA = 3.3 V, TA = 25 ℃.

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**5.** **Package information**

**5.1.**

**BGA176 package outline dimensions**

**Figure 5-1. BGA176 package outline**

aaa B

2X

E

B A

E1

eee C A B

fff C

PIN 1 CORNER e b

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 PIN 1 CORNER

A B C D E F G

LASER MARK

PIN 1

A B C D E F G

e

H J K L M

D

H J K L M

D1

N P R

L

N P R

aaa A L

2X

TOP VIEW BOTTOM VIEW

DETAIL A A2 A3

ccc C

SEATING PLANE

SEATING PLANE A ddd C A1 c C

C

SIDE VIEW DETAIL A(3:1)

**Table 5-1. BGA176 package dimensions**

|  |  |  |  |
| --- | --- | --- | --- |
| Symbol | Min | Typ | Max |
| A | — | — | 0.89 |
| A1 | 0.13 | 0.18 | 0.23 |
| A2 | 0.58 | 0.63 | 0.68 |
| A3 | — | 0.45 | — |
| b | 0.20 | 0.25 | 0.30 |
| c | 0.15 | 0.18 | 0.21 |
| D | 9.90 | 10.00 | 10.10 |
| D1 | — | 9.10 | — |
| E | 9.90 | 10.00 | 10.10 |
| E1 | — | 9.10 | — |
| e | — | 0.65 | — |
| L | — | 0.325 | — |
| aaa | — | 0.10 | — |
| ccc | — | 0.20 | — |
| ddd | — | 0.08 | — |
| eee | — | 0.15 | — |
| fff | — | 0.08 | — |

(Original dimensions are in millimeters)

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**Figure 5-2. BGA176 recommended footprint**

Dimension Recommended values

Pitch 0.65 mm

Dpad 0.30 mm

Dsm 0.40 mm

Dpad

Dsm

(Original dimensions are in millimeters)

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**5.2.**

**LQFP144 package outline dimensions**

**Figure 5-3. LQFP144 package outline**

A3

c

F A1 A2A θ 0.08

D

D1

108 73

109 72 0.25

L

L1

DETAIL: F

E1 E

b

b1

c1 c

144 37 BASE METAL

1

b

e

B B

36

WITH PLATING

SECTION B-B

**Table 5-2. LQFP144 package dimensions**

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Min** | **Typ** | **Max** |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 21.80 | 22.00 | 22.20 |
| D1 | 19.90 | 20.00 | 20.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| e | — | 0.50 | — |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

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**Figure 5-4. LQFP144 recommended footprint**

22.70

20.30

1

36

108

73

1.20

0.50

(Original dimensions are in millimeters)

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**5.3.**

**BGA100 package outline dimensions**

**Figure 5-5. BGA100 package outline**

aaa B

2X E B A E1 eee C A B

PIN 1 CORNER

e

b

fff C

PIN 1 CORNER

1 2 3 4 5 6 7 8 9 10 11 12 12 11 10 9 8 7 6 5 4 3 2 1

A

B

LASER MARK

PIN 1

A

B

C D E

C D E

e

F G H J

D

F G H J

D1

K L M

L

K L M

aaa A L

2X

TOP VIEW BOTTOM VIEW

A2

DETAIL A

ccc C A3

SEATING PLANE A c

C 100X ddd C A1 SEATING PLANE C

SIDE VIEW DETAIL A(3:1)

**Table 5-3. BGA100 package dimensions**

|  |  |  |  |
| --- | --- | --- | --- |
| Symbol | Min | Typ | Max |
| A | — | — | 0.84 |
| A1 | 0.13 | 0.18 | 0.23 |
| A2 | 0.53 | 0.58 | 0.63 |
| A3 | — | 0.40 | — |
| b | 0.20 | 0.25 | 0.30 |
| c | 0.15 | 0.18 | 0.21 |
| D | 6.90 | 7.00 | 7.10 |
| D1 | — | 5.50 | — |
| E | 6.90 | 7.00 | 7.10 |
| E1 | — | 5.50 | — |
| e | — | 0.50 | — |
| L | — | 0.625 | — |
| aaa | — | 0.10 | — |
| ccc | — | 0.20 | — |
| ddd | — | 0.08 | — |
| eee | — | 0.15 | — |
| fff | — | 0.08 | — |

(Original dimensions are in millimeters)

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**Figure 5-6. BGA100 recommended footprint**

Dimension Recommended values

Pitch 0.50 mm

Dpad 0.25 mm

Dsm 0.35 mm

Dpad

Dsm

(Original dimensions are in millimeters)

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**5.4.**

**LQFP100 package outline dimensions**

**Figure 5-7. LQFP100 package outline**

A3 A2 A θ c

F A1 0.08

eB

D

D1

75 51

0.25

76 50

L

L1

DETAIL: F

E1 E

b

b1

100 26 c1 c

BASE METAL

b

1

e

B

B

25

WITH PLATING

SECTION B-B

**Table 5-4. LQFP100 package dimensions**

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Min** | **Typ** | **Max** |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.10 |
| e | — | 0.50 | — |
| eB | 15.05 | — | 15.35 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

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**Figure 5-8. LQFP100 recommended footprint**

16.70

14.30

1

25

75

51

1.20

0.50

(Original dimensions are in millimeters)

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**5.5.**

**Thermal characteristics**

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “θ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θJA: Thermal resistance, junction-to-ambient. θJB: Thermal resistance, junction-to-board. θJC: Thermal resistance, junction-to-case.

ᴪJB: Thermal characterization parameter, junction-to-board.

ᴪJT: Thermal characterization parameter, junction-to-top center.

θJA=(TJ-TA)/PD (5-1)

θJB=(TJ-TB)/PD (5-2)

θJC=(TJ-TC)/PD (5-3)

Where, TJ = Junction temperature. TA = Ambient temperature

TB = Board temperature

TC = Case temperature which is monitoring on package surface PD = Total power dissipation

θJA represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θJA can be considerate as better overall thermal performance. θJA is generally used to estimate junction temperature.

θJB is used to measure the heat flow resistance between the chip surface and the PCB board.

θJC represents the thermal resistance between the chip surface and the package top case. θJC is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

**Table 5-5. Package thermal characteristics(1)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Condition** | **Package** | **Value** | **Unit** |
| θJA | Natural convection, 2S2P PCB | BGA176 | 45.02 | °C/W |
| LQFP144 | 48.76 |
| BGA100 | 78.32 |
| LQFP100 | 57.42 |
| θJB | Cold plate, 2S2P PCB | BGA176 | 26.55 | °C/W |
| LQFP144 | 35.00 |
| BGA100 | 55.27 |

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **Condition** | **Package** | **Value** | **Unit** |  |
|  |  | LQFP100 | 31.68 |  |
| θJC | Cold plate, 2S2P PCB | BGA176 | 9.93 | °C/W |
| LQFP144 | 12.03 |
| BGA100 | 20.15 |
| LQFP100 | 13.85 |
| ᴪJB | Natural convection, 2S2P PCB | BGA176 | 28.31 | °C/W |
| LQFP144 | 35.32 |
| BGA100 | 55.74 |
| LQFP100 | 41.28 |
| ᴪJT | Natural convection, 2S2P PCB | BGA176 | 0.69 | °C/W |
| LQFP144 | 1.86 |
| BGA100 | 1.74 |
| LQFP100 | 0.75 |

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

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**6.**

**Ordering information**

**Table 6-1. Part ordering code for GD32F470xx devices**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Ordering code** | **Flash (KB)** | **Package** | **Package type** | **Temperature**  **operating range** |
| GD32F470IKH6 | 3072 | BGA176 | Green | Industrial  -40°C to +85°C |
| GD32F470IIH6 | 2048 | BGA176 | Green | Industrial  -40°C to +85°C |
| GD32F470IGH6 | 1024 | BGA176 | Green | Industrial  -40°C to +85°C |
| GD32F470ZKT6 | 3072 | LQFP144 | Green | Industrial  -40°C to +85°C |
| GD32F470ZIT6 | 2048 | LQFP144 | Green | Industrial  -40°C to +85°C |
| GD32F470ZGT6 | 1024 | LQFP144 | Green | Industrial  -40°C to +85°C |
| GD32F470ZGT7 | 1024 | LQFP144 | Green | Industrial  -40°C to +105°C |
| GD32F470ZET6 | 512 | LQFP144 | Green | Industrial  -40°C to +85°C |
| GD32F470VKH6 | 3072 | BGA100 | Green | Industrial  -40°C to +85°C |
| GD32F470VIH6 | 2048 | BGA100 | Green | Industrial  -40°C to +85°C |
| GD32F470VGH6 | 1024 | BGA100 | Green | Industrial  -40°C to +85°C |
| GD32F470VGH7 | 1024 | BGA100 | Green | Industrial  -40°C to +105°C |
| GD32F470VKT6 | 3072 | LQFP100 | Green | Industrial  -40°C to +85°C |
| GD32F470VIT6 | 2048 | LQFP100 | Green | Industrial  -40°C to +85°C |
| GD32F470VIT7 | 2048 | LQFP100 | Green | Industrial  -40°C to +105°C |
| GD32F470VGT6 | 1024 | LQFP100 | Green | Industrial  -40°C to +85°C |
| GD32F470VGT7 | 1024 | LQFP100 | Green | Industrial  -40°C to +105°C |
| GD32F470VET6 | 512 | LQFP100 | Green | Industrial  -40°C to +85°C |

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**7.**

**Revision history**

**Table 7-1. Revision history**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Revision No.** | **Description** | | | | | | **Date** |
| 1.0 | Initial Release | | | | | | Feb.22, 2022 |
| 1.1 | 1. Add  ***circuit***  2. Add  3. Modify  ***Package***  4. Mofidy  5. Modify  6. Modify  ***memory***  7. Modify  ***4-11.*** | ***Figure 4-1. Recommended PDR\_ON pin*** | | | | | May.24, 2022 |
| **i**n chapter  ***characteristics***.  description of  ***characteristics***.  the BGA100  ***information***  the I2C  ***characteristics***.  fsck maximum  ***characteristics(1)***.  the erase  ***characteristics***  the value of  ***ESD characteristics*** | | ***4.5. Power supply supervisor*** | | |
| EMI in chapter ***4.4. EMC***  footprint parameters in  .  timing parameters in  value in ***Table 4-37.***  cycles in ***Table 4-24. Flash***  .  VESD(HBM) and VESD(CDM)  ***(1)***. | chapter ***5.***  ***4.16. I2C*** | |
| ***USART***  in ***Table*** | |
| 1.2 | 1. Update  ***4-24.***  2. Update  3. Update  ***pin circuit***  4. Update | | ***Table 4-37 USART characteristics(1)***, ***Flash memory characteristics***.  ***Table 4-11. ESD characteristics(1)***.  ***Figure 4-2. Recommended external*** | | | ***Table*** | Jul.12, 2022 |
| ***NRST*** |
| ***(1)***.  ***Table 4-35. Standard SPI characteristics(1)***. | | | |
| 1.3 | 1. Add GD32F470xxT7 related descriptions. | | | | | | Aug.22, 2022 |
| 1.4 | 1. Add notes for ***Table 4-2. DC operating conditions***  and ***Table 4-7. Power consumption characteristics(2)(3)(4)(5)(6)***, and update ***Table 4-7. Power consumption characteristics(2)(3)(4)(5)(6)***.  2. Update ***Table 4-25. Flash memory***  ***characteristics(1)***.  3. Add description of EMI and ***Table 4-10. EMI***  ***characteristics(1)***.  4. Update ***Figure 4-7. I2C bus timing diagram***.  5. Update ***Figure 4-26. I/O port DC***  ***characteristics(1)(3)***. | | | | | | Jan.4, 2023 |
| 1.5 | 1. Add GD32F470VGH7. | | | | | | Feb.21, 2023 |
| 1.6 | 1. Add the ***Table 4-44. Dynamics characteristics:***  ***Ethernet MAC signals for SMI(1)*** and ***Figure 4-12.*** | | | | | | Mar.14, 2023 |

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|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Revision No.** | **Description** | | | | | | | **Date** |
|  | ***Ethernet SMI timing diagram***. | | | | | | |  |
| 1.7 | 1. Update ***Table***  ***definitions***, ***definitions***, ***definitions***, ***definitions supply*** | | ***2-3. GD32F470Ix BGA176 pin***  ***Table 2-4. GD32F470Zx LQFP144 pin*** | | | | | Jul.8, 2023 |
| ***Table 2-5. GD32F470Vx BGA100 pin***  ***Table 2-6. GD32F470Vx LQFP100 pin*** | | | | |
| ***decoupling*** | and ***Figure 4-1. Recommended power*** | | | |
| ***capacitors(1)(2)***. | | | |
| 1.8 | 1. Modify the PECYC to 100 kcycles in ***Table 4-24.***  ***Flash memory characteristics(1)***.  2. Modify description note(3) of ***Table 4-26. I/O port***  ***DC characteristics(1)(3)***.  3. Add device GD32F470VIT7. | | | | | | | Dec.27, 2023 |
| 1.9 | 1. Delete EXMC pin in GD32F470Vx. | | | | | | | Apr.18, 2024 |
| 2.0 | 1. Modify ***Table 4-27. I/O port DC characteristics***  2. Modify ***Figure 5-1. LQFP144 package outline***  ***Figure 5-5. LQFP100 package outline*** and  ***5-7. LQFP64 package outline***.  3. Modify ***Table 4-5. Start-up timings of Operating***  ***conditions(1)(2)(3)***. | | | | | | ***(1)(3)***.  ,  ***Figure*** | Jul.15, 2024 |
|  |
| 2.1 | 1. 2. 3.  4.  5.  6. | Update the note on VREFP ***Table 4-28. ADC characteristic*** Modify DAC to DAC0 in chapter ***overview***.  Update the parameters fPLLOUT ***PLL characteristic***, ***Table 4- characteristic*** and ***Table 4-22 characteristic***.  Update ***Figure 4-4. Recommended circuit*** and note.  Update description in chapter ***interface*** and  ***synchronous/asynchronous*** | | | power up  .  ***2. Device***  and fVCO in  ***21. PLLI2S . PLLSAl***  ***3.13. Serial*** | timing in  ***-***  ***Table 4-20.*** | | Jan. 23, 2025 |
| ***PDR\_ON pin***  ***peripheral*** | |
| ***3.14*** ***Universal*** | | |
| ***receiver transmitter*** | | |
| ***(USART/UART)***.  Update the descripton of th(DATA) in ***Table 4-54.***  ***DCI characteristics(1)***. | | | | | |

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